DEPARTMENT OF ELECTRONICS
&TELECOMMUNICATION ENIGINEERING

SEMESTER:V

LECTURES NOTES

Subject: VLSI & EMBEDDED SYSTEM

Unit-1
Introduction to VLSI

Historical Perspective

The electronics industry has achieved a phenomenal growth over the last few decades,mainly due to the rapid advances in integration technologies and large-scale systems design.Theuseofintegratedcircuitsinhigh-performance computing,telecommunications,andconsumerelectronicshasbeengrowingataveryfastpace. Typically,therequiredcomputational and information processing power of these applications is the driving force forthe fast development of this field. Figure 1 gives an overview of the prominent trends ininformation technologies over the next decade. The current leading edge technologies (such aslowbit-rate videoandcellular communications) already providethe end-usersacertainamount of processing power and portability.This trend is expected to continue,with veryimportantimplicationsforVLSIandsystemsdesign.Oneofthemostimportantcharacteristics of information services is their increasing need for very high processing powerandbandwidth (in order to handle real-timevideo,forexample).

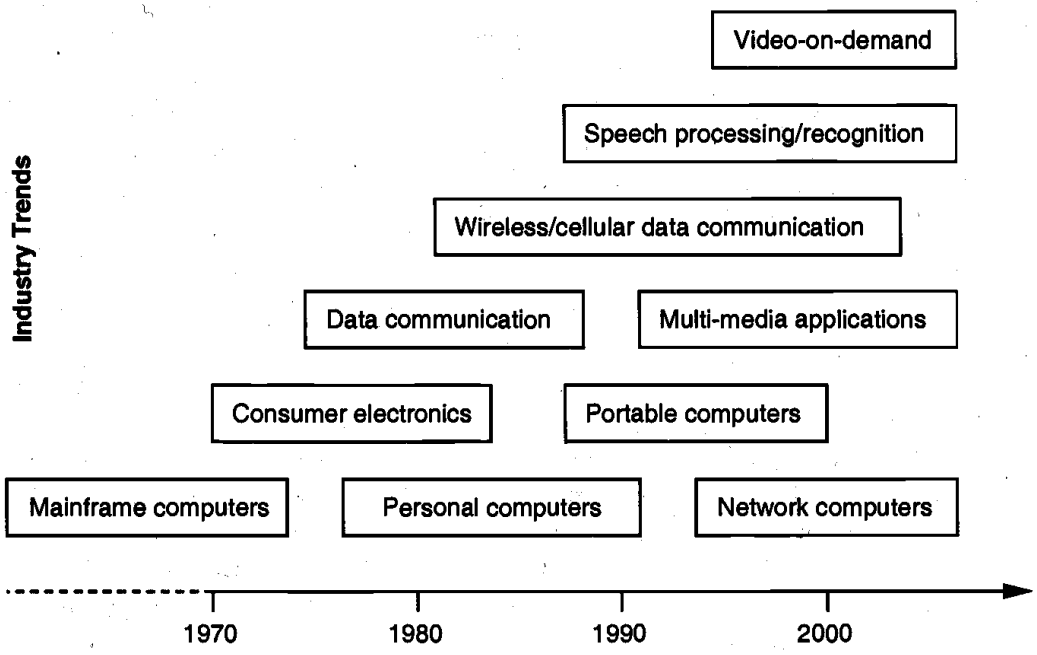


FIG.1(Prominent"driving"trends in information service technologies.)

ERA	DATE	COMPLEXITY (# of logic blocks per chip)
Single transistor	1958	< 1
Unit logic (one gate)	1960	1
Multi-function	1962	2 - 4
Complex function	1964	5 - 20
Medium Scale Integration (MSI)	1967	20 - 200
Large Scale Integration (LSI)	1972	200 - 2,000
Very Large Scale Integration (VLSI)	1978	2,000 - 20,000
Ultra Large Scale Integration (ULSI)	1989	20,000 - ?

VLSI DESIGN METHODOLOGIES AND VLSI DESIGN FLOW

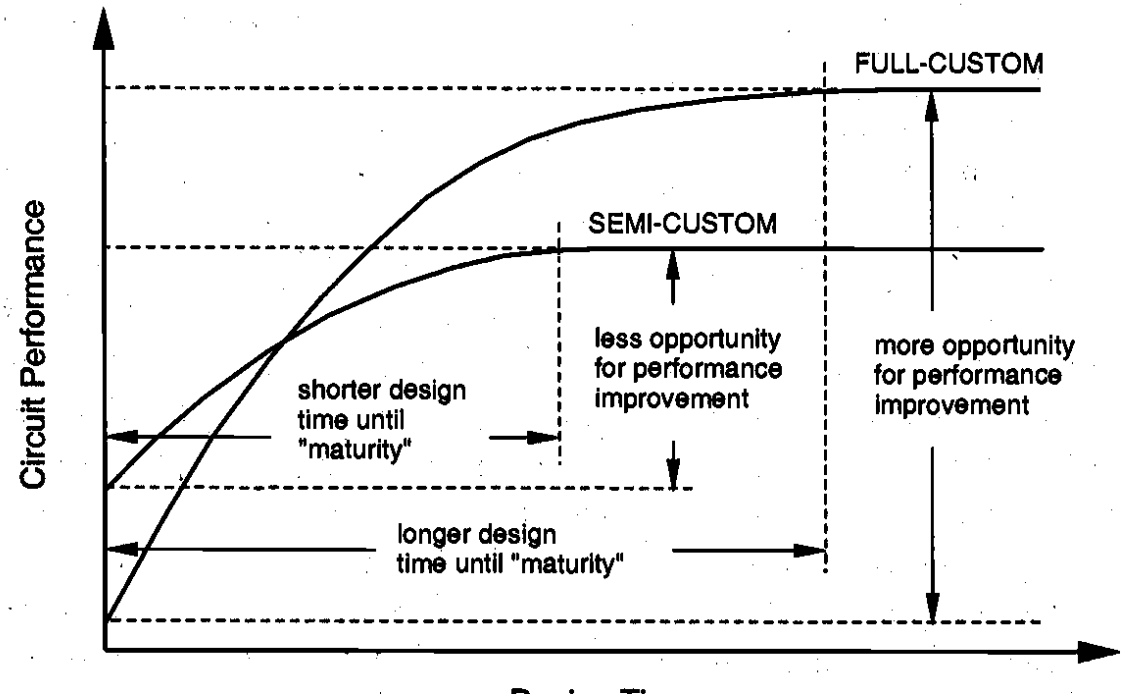
VLSI DESIGN METHODOLOGIES

The demands of the rapidly rising chip complexity has created significant challenges in many areas; practically hundreds of team members are involved in the development of a typical VLSI product,including the development of technology,computer-aided design(CAD) tools, chip design, fabrication, packaging, testing and reliability qualification. The level of circuit performance which can be reached within a certain design time strongly depends on the efficiency of the design methodologies, as well as on the design style two different VLSI design styles are compared for their relative merits in the design of the same product.

1. FULL CUSTOM DESIGN
2. SEMI CUSTOM DESIGN

FULL CUSTOM DESIGN - Using the full-custom design style (where the geometry and the placement of every transistor can be optimized individually) requires a longer time until design maturity can be reached, yet the inherent flexibility of adjusting almost every aspect of circuit design allows far more opportunity for circuit performance improvement during the design cycle.The final

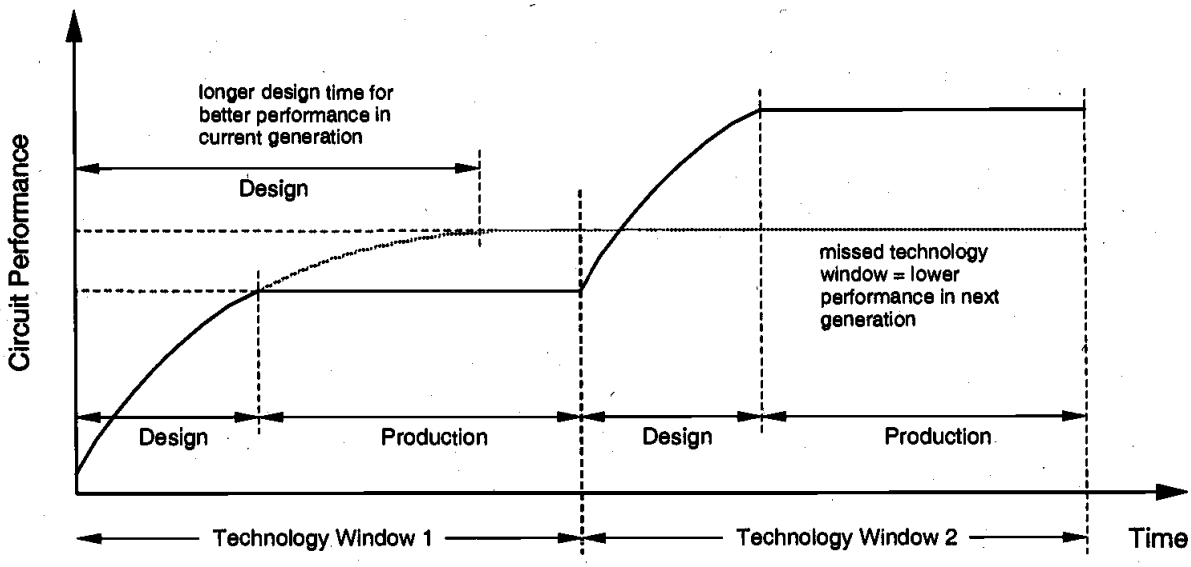
product typically has a high level of performance (e.g. high processing speed, low power dissipation) and the silicon area is relatively small because of better area utilization.Butth is comes at a larger cost in terms of design time.



(Impact of different VLSI design styles upon the design cycle time and the achievable circuit performance).

SEMI-CUSTOM DESIGN -Using a semi-custom design style (such as standard-cell based design or FPGA) will allow a shorter design time until design maturity can beachieved. In the early design phase, the circuit performance can be even higher than that of a full-custom design, since some of the components used in semi-custom design are already optimized.But the semi-custom design style offers less opportunity for performance improvement over the long run,and the overall performance of the final product will inevitably be less than that of a full-custom design.

In addition to the proper choice of a VLSI design style, there are other issues whichmust be addressed in view of the constantly evolving nature of the VLSI manufacturingtechnologies. Approximately every two years, a new generation of technology is introduced,which typically allows for smaller device dimensions and consequently, higher integration density and higher performance.



. (Progressive performance improvement of a VLSI product)

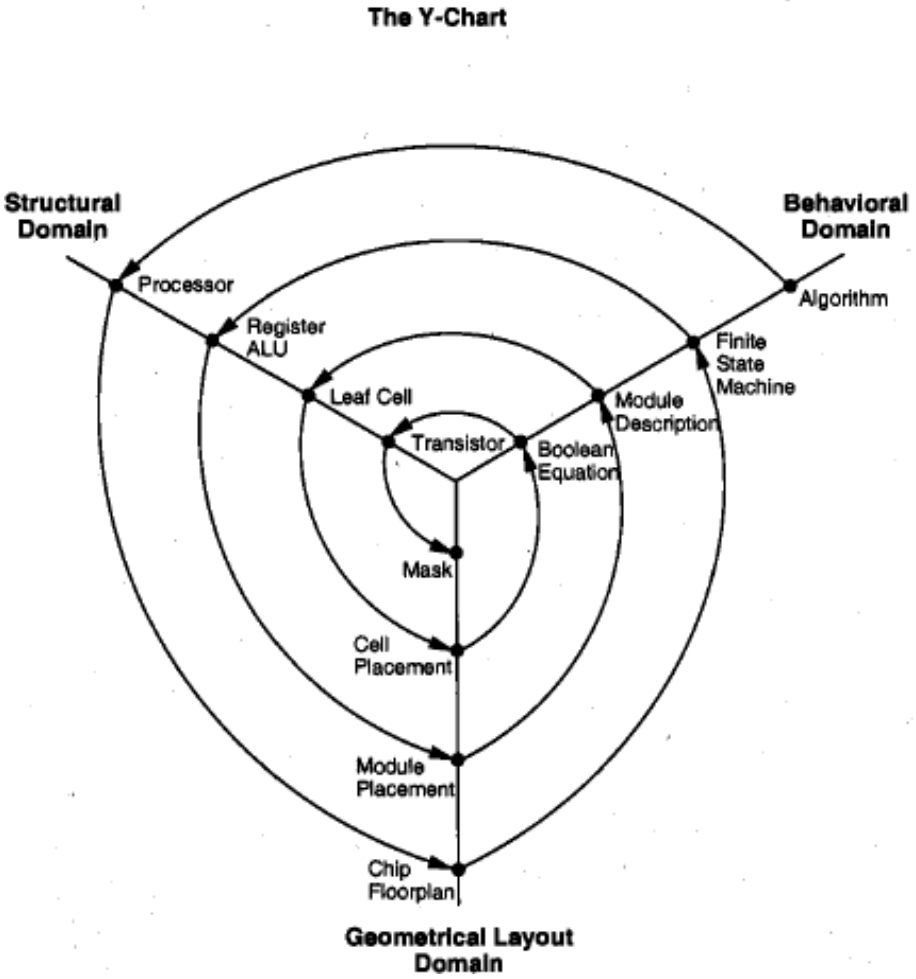
VLSI Design Flow

The design process, at various levels, is usually evolutionary in nature. It starts with a given set of requirements. Initial design is developed and tested against the requirements.When requirements are not met, the design has to be improved. If such improvement is eithernot possible or too costly, then a revision of requirements and an impact analysis must be considered. The Y-chart (first introduced by D. Gajski) shown in Fig. 4 illustrates a design flow for most logic chips, using design activities on three different axes (domains) which resemble the letter "Y."

TheY-chart consists of three domains of representation,namely

(i)behavioural domain,

(ii) structural domain, and (iii) geometrical layout domain. The design flow starts from the algorithm that describes the behavior of the target chip.The corresponding architecture of the processor is first defined.It is mapped on to the chip surface by floor planning.The next design evolution in the behavioral domain defines finite state machines(FSMs)which are structurally implemented with functional modules such as registers and arithmetic logic units (ALUs). These modules are then geometrically placed onto the chip surface using CAD tools for automatic module placement followed by routing,with a goal of minimizing the interconnects area and signal delays. The third evolution starts with a behavioral module description. Individual modules are then implemented with leaf cells. At this stage the chip is described in terms of logic gates (leaf cells), which can be placed and interconnected by using a cell placement and routing program.



.Typical VLSI design flow in three domains(Y-chart representation).

The last evolution involves a detailed Boolean description of leaf cells followed by a transistor level implementation of leaf cells and mask generation. In the standard cell based design style, leaf cells are pre designed (at the transistor level) and stored in a library for logic implementation, effectively eliminating the need for the transistor level design. Figure 4provides a more simplified view of the VLSI design flow, taking into account the various representations,or abstractions of design:behavioral,logic,circuit and mask layout.Notethat the verification of design plays a very important role in every step during this process.The failure to properly verify a design in its early phases typically causes significant andexpensivere-design ata later stage,which ultimatelyincreases the time-to-market.

Full-CustomMaskLayoutDesign

In this section, the basic mask layout principles for CMOS inverters and logic gateswill be presented. The design of physical layout is very tightly linked to overall circuitperformance(area,speed,andpowerdissipation)sincethephysicalstructuredirectlyd etermines the trans-conductance of the transistors, the parasitic capacitances and resistances,and obviously, the silicon area which is used for a certain function. On the other hand, thedetailed mask layout of logic gates requires a very intensive and time consuming designeffort,whichisjustifiableonlyinspecialcircumstanceswherethe areaand/ortheperfor manceofthecircuitmustbeoptimizedunderverytightconstraints.Therefore,automated layout generation (e.g., using a standard cell library, computer aided placement-and-routing) is typically preferred for the design of most digital VLSI circuits. In order tojudge the physical constraints and limitations, however, the VLSI designer must also have agoodunderstandingof thephysical mask layout process.

MOS Transistor

.TheMetalOxideSemiconductor(MOS)Structure

We will start our investigation by considering the electrical behavior of the simpletwo-. terminal MOS structure shown in Fig. 3.1. Note that the structure consists of threelayers: The metalgate electrode, the insulating oxide (SiO2) layer, and the p-type bulksemiconductor (Si), called the substrate. As such, the MOS structure forms a capacitor, withthe gate and the substrate acting as the two terminals (plates) and the oxide layer as thedielectric. The thickness of the silicon dioxide layer is usually between 10nm and 50 nm.The carrier concentration and its local distribution within the semiconductor substrate can now be manipulated by the external voltages applied to the gate and substrate terminals. Abasic understanding of the bias conditions for establishing different carrier concentrations in the substrate will also provide valuable insight into the operating conditions of more complicated MOSFET structures.

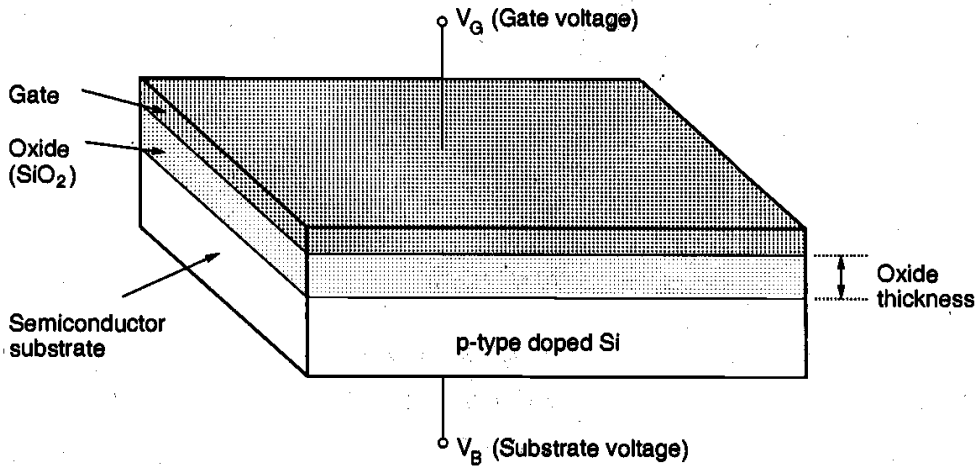


Figure 3.1. Two-terminal MOS structure.

Consider first the basic electrical properties of the semiconductor (Si) substrate, which acts as one of/the electrodes of the MOS capacitor. The equilibrium concentrations of mobile carriers in a semiconductor always obey the *Mass Action Law*

$$n \cdot p = n_i^2 \qquad (3.1)$$

given by

Here n and p denote the mobile carrier concentrations of electrons and holes,respectively,and n_i denotes the intrinsic carrier concentration of silicon,which is a function

ofthetemperatureT.Atroomtemperature,i.e.,T=300Kni isapproximatelyequalto1.45x 1010 cm-3. Assuming that the substrate is uniformly doped with an acceptor (e.g., Boron)concentration NA, the equilibrium electron and hole concentrations in the p-type substrate areapproximated by

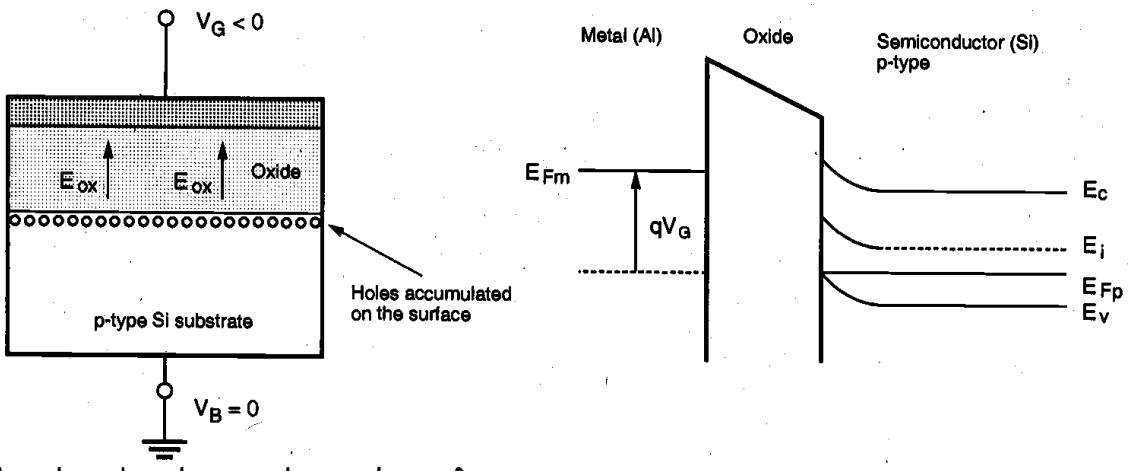
$$n_{po} \cong \frac{n_i^2}{N_A}$$
$$p_{po} \cong N_A \qquad (3.2)$$

ThedopingconcentrationNA is typicallyontheorderof 1015to1016cm-3; thus,it much

isgreaterthan the intrinsiccarrier concentration,

The MOS System under External Bias

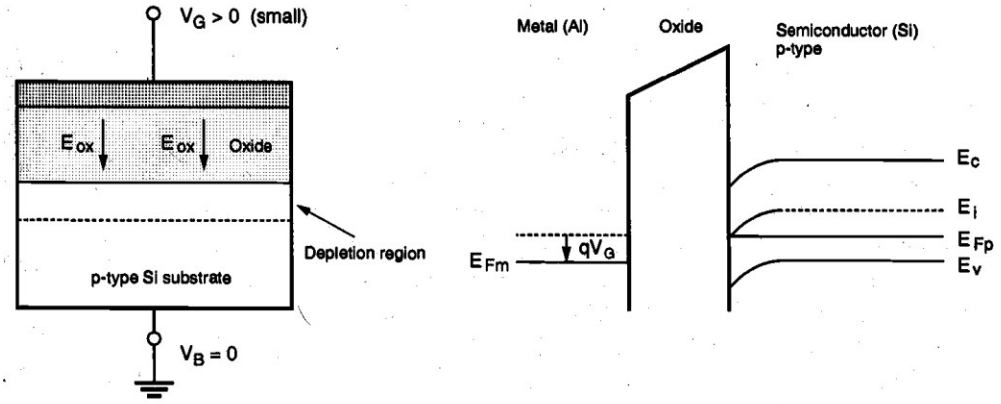
We now turn our attention to the electrical behavior of the MOS structure underexternally applied bias voltages. Assume that thesubstrate voltage is set at VB = 0, and letthe gate voltage be the controlling parameter. Depending on the polarity and the magnitude ofVG, three different operating regions can be observed for the MOS system: accumulation,depletion, and inversion. If a negative voltage VG is applied to the gate electrode, the holes inthe p-type substrate are attracted to the semiconductor-oxide interface. The majority carrierconcentration near the surface becomes larger than the equilibrium hole concentration in thesubstrate; hence, this condition is called carrier accumulation on the surface (Fig. 3.5). Notethat in this case, the oxide electric field is directed towards the gate electrode. The negativesurfacepotential also causesthe



energybands to bend upward nearthesurface.

Figure3.5. Thecross-sectional viewand theenergyband diagramof theMOS structure

While the hole density near the surface increases as a result of the applied negativegate bias, the electron (minority carrier) concentration decreases as the negatively chargedelectronsarepusheddeeperinto thesubstrateoperatingin accumulation



$$dQ = -q \cdot N_A \cdot dx \tag{3.7}$$

The *change* in surface potential required to displace this charge sheet dQ by a distance x_d away from the surface can be found by using the Poisson equation.

$$d\phi_s = -x \cdot \frac{dQ}{\varepsilon_{Si}} = \frac{q \cdot N_A \cdot x}{\varepsilon_{Si}} dx \tag{3.8}$$

Integrating (3.7) along the vertical dimension (perpendicular to the surface) yields

$$\int_{\phi_F}^{\phi_s} d\phi_s = \int_0^{x_d} \frac{q \cdot N_A \cdot x}{\varepsilon_{Si}} \, dx \tag{3.9}$$

$$\phi_s - \phi_F = \frac{q \cdot N_A \cdot x_d^2}{2\,\varepsilon_{Si}} \tag{3.10}$$

Thus, the depth of the depletion region is

$$x_d = \sqrt{\frac{2\varepsilon_{Si} \cdot |\phi_s - \phi_F|}{q \cdot N_A}} \tag{3.11}$$

and the depletion region charge density, which consists solely of fixed acceptor ions in this region, is given by the following expression

$$Q = -q \cdot N_A \cdot x_d = -\sqrt{2q \cdot N_A \cdot \varepsilon_{Si} \cdot |\phi_s - \phi_F|} \tag{3.12}$$

region.

Now consider the next case in which a small positive gate bias VG is applied to thegate electrode.Since the substrate biasiszero,the oxide electric fieldwillbe directedtowards the substrate in this case. The positive surface potential causes the energy bands tobend downward near the surface, as shown in Fig. 3.6. The majority carriers, i.e., the holes inthe substrate, will be repelled back into the substrate as a result of the positive gate bias, andthese holes will leave negatively charged fixed acceptor ions behind. Thus, a depletion regioniscreatednearthesurface.Notethatunderthisbiascondition,theregionnearthesemiconductor-oxideinterfaceis nearlydevoid ofall mobile carriers.

To complete our qualitative overview of different bias conditions and their effectsupon the MOS system, consider next a further increase in the positive gate bias. As a result ofthe increasing surface potential, the downward bending of the energy bands will increase aswell. Eventually, the mid-gap energy level Ei becomes smaller than the Fermi level EFP onthe surface, which means that the substrate semiconductor in this region becomes n-type.Within this thin layer, the electron density is larger than the majority hole density, since thepositive gate potential attracts additional minority carriers (electrons) from the bulk substratetothesurface(Fig. 3.7).

$$x_{dm} = \sqrt{\frac{2 \cdot \varepsilon_{Si} \cdot |2\phi_F|}{q \cdot N_A}} \qquad (3.13)$$

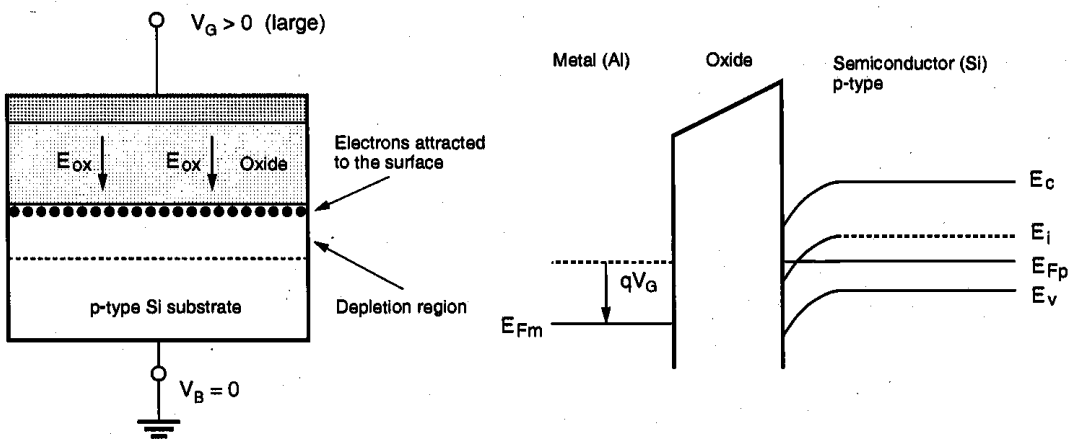


Figure 3.7. The cross-sectional view and the energy band diagram of the MOS structure in surface inversion, under larger gate bias voltage.

The n-type region created near the surface by the positive gate bias is called theinversion layer, and this condition is called surface inversion. It will be seen that the thininversion layer on the surface with a large mobile electron concentration can be utilized forconductingcurrentbetweentwoterminalsoftheMOStransistor.Thecreationofaconductingsurfaceinversionlayerthroughexternallyappliedgatebiasisanessentialphenomenon for current conduction in MOS transistors. In the following we will examine thestructureand the operationofthe MOSField Effect Transistor(MOSFET).

MOSFET Current-Voltage Characteristics

The analytical derivation of the MOSFET current-voltage relationships for various bias conditions requires that several approximations be made to simplify the problem.

Without these simplifying assumptions,analysis of the actual three-dimensional MOS system would become a very complex task and would prevent the derivation of closedformcurrent-voltageequations.Inthe'following,wewillusethe*gradualchannelapproximation* (GCA) for establishing the MOSFET current-voltage relationships, which will effectively reduce the analysis to a one-dimensional current-flow problem. This will allow us to devise relatively simple current equations that agree well with experimental results. As in every approximate approach, however, the GCA also has its limitations, especially for small-

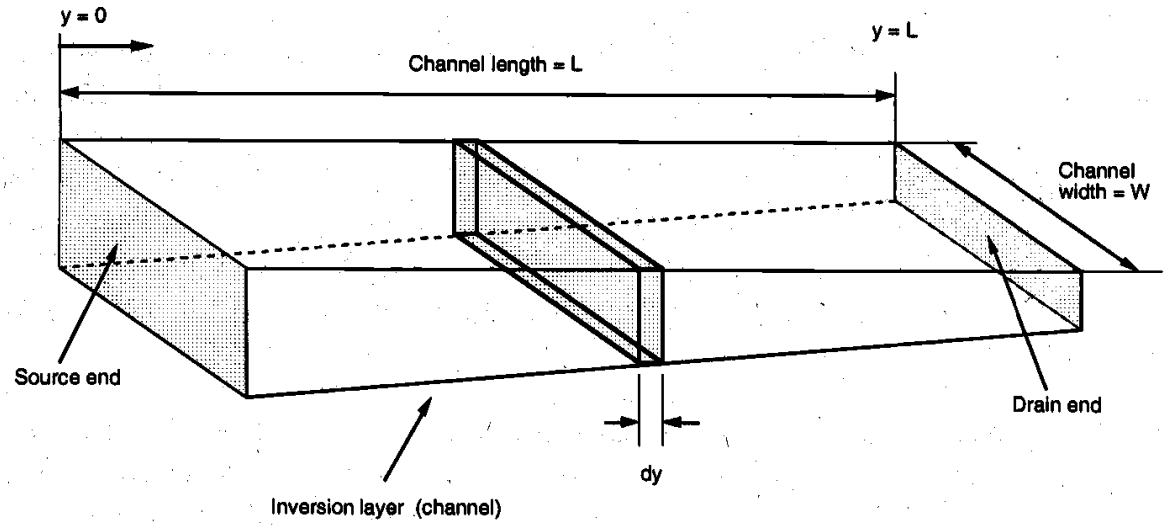


Figure 3.16. **Simplified geometry of the surface inversion layer (channel region).**

geometry MOSFETs. We will investigate the most significant limitations and examine

some of the possible remedies.

Now consider the incremental resistance *dR* of the differential channel segment Assuming that all mobile electrons in the inversion layer have a constant

Surface mobility jun,the incremental resistance can be expressed as follows.Note that the minus sign is due to the negative polarity of the inversion layer charge Q_I.

$$dR = -\frac{dy}{W \cdot \mu_n \cdot Q_I(y)} \quad \text{.....(1)}$$

The *electron surface mobility yun* used , depends on the doping concentration of the channel region, and its magnitude is typically about one-half of that of the bulk electron mobility. We will assume that the channel current density is uniform across this segment.According to our one-dimensional model, the channel (drain) current *ID* flows between the source and the drain regions in the y-coordinate direction. Applying Ohm's law for this segment yields the voltage drop along the incremental segment *dy,* in the y direction.

$$dV_c = I_D \cdot dR = -\frac{I_D}{W \cdot \mu_n \cdot Q_I(y)} \cdot dy \quad \text{.....(2)}$$

th
e This equation can now be integrated along the channel,i.e., from y=0toy=L,using

boundary conditions given in above equation

$$\int_0^L I_D \cdot dy = -W \cdot \mu_n \int_0^{V_{DS}} Q_I(y) \cdot dV_c \quad \text{.....(3)}$$

The left-hand side of this equation is simply equal to LID.The integral on the right-hand side is evaluated by replacing Q_I in

$Q_I(y)=-Cox[VGSvVC(Y)-VT0]$

$$I_D = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot (V_{GS} - V_{T0}) V_{DS} - V_{DS}^2\right]$$

Equation(3.32)represents the drain current ID as a simple second-order function of two external voltages,VGS and VDS.This current equation can also be rewritten as

$$I_D = \frac{k}{2}\cdot[k' = \mu_n \cdot C_{ox}{}^{\prime 0})V_{DS} - V_{DS}^2]$$

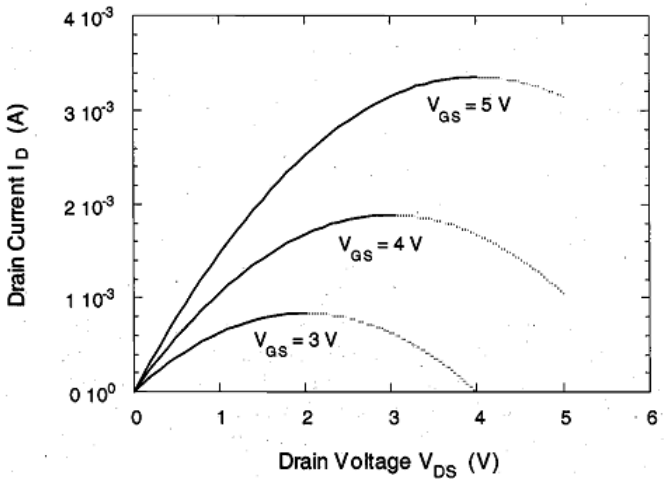
.....(5)where the parameters k and k' are

$$k = k' \cdot \frac{W}{L}$$

defined as

.....(6)

The drain current equation given in (5)is the simple st analytical approximation for the MOSFET current-voltage relationship.Note that, in addition to the process dependent constants k' and V,the current-voltage relationship is also affected by the device dimensions,W and L. In fact, we will see that the ratio of WIL is one of the most important design parameters in MOS digital circuit design. Now, we must determine the region of validity for this equation and what his means for the practical use of the



equation.

The drain current-drain voltage curves shown above reach their peak value for VDS =VGS- VT0 Beyond this maximum, each curve exhibits a negative differential conductance,which is not observed in actual MOSFET current-voltage measurements

(section shown by the dashed lines).We must remember now that the drain current equation(4) has been derived under the following voltage assumptions,

$$V_{GS} \geq V_{T0}$$
$$V_{GD} = V_{GS} - V_{DS} \geq V_{T0}$$

$$V_{DS} \geq V_{DSAT} = V_{GS} - V_{T0}$$

Also, drain current measurements with constant V_S show that the current I_D does not show much variation as a function of the drain voltage. V_{DS} beyond the saturation boundary,but rather remains approximately constant around the peak value reached for V_{DS}= VD_{SAT} This saturation drain current level can be found simply by substituting(7)for

$$I_D(sat) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot (V_{GS} - V_{T0}) \cdot (V_{GS} - V_{T0}) - (V_{GS} - V_{T0})^2\right]$$
$$= \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{T0})^2$$

.....(8)

Thus, the drain current ID becomes a functiononly of the gate-to-source voltage VGS,beyond the saturation boundary.Note that this constant saturation current approximation is not very accurate in reality, and that the saturation-region drain current continues to have a certain dependence on the drain voltage. For simple hand calculations,however,(8) provides a sufficiently accurate approximation of the MOSFET drain (channel)current in saturation.

Explain MOSFET capacitances.

The majority of the topics covered in this chapter has been related to the steady -statebehaviorofthe MOStransistor.Thecurrent-voltagecharacteristicsinvestigatedherecanbe

Applied for investigating the DC response of MOS circuits under various operating conditions.

the gate electrode overlaps both the source region and the drain region at the edges.The two overlap capacitances that arise as a result of this structural arrangement are called CGD (overlap) and CGS (overlap), respectively. Assuming that both the source and the drain diffusion regions have the same width W, the overlap capacitances can be found as

$$C_{GS}(overlap) = C_{ox} \cdot W \cdot L_D$$
$$C_{GD}(overlap) = C_{ox} \cdot W \cdot L_D$$

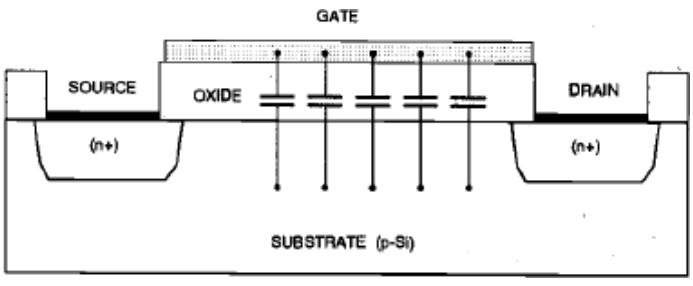
$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

Note that both of the se overlap capacitances do not depend on the bias conditions, i.e., they are voltage-independent. Now consider the capacitances which result from the interaction between the gate voltage and the channel charge. Since the channel region is connected to the source,the drain,and the substrate,we can identify three capacitances between the gate and these regions, i.e., Cgs, C d and C b respectively. Notice that in reality, the gate-to-channel capacitance is distributed and voltage-dependent. Then, the gate-to-source capacitance Cgs is actually the gate-to-channel capacitance seen between the gate and the source terminals; the gate-to-drain capacitance C ad is actually the gate-to-channel capacitance seen between the gate and the drain terminals. A simplified view of their bias-dependence can be obtained by observing the conditions in the channel region during cut-off, linear, and saturation modes.

In cut-off mode (Fig. (a)), the surface is not inverted. Consequently, there is no conducting channel that links the surface to the source and to the drain. Therefore, the gate-to-source and the gate-to-drain capacitances are both equal to zero: Cgs = Cgd= 0. The gate-to-substrate capacitance can be approximated by

$$C_{gb} = C_{ox} \cdot W \cdot L$$

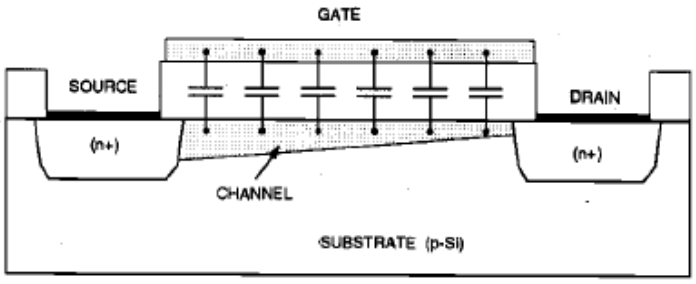
(a)



In linear-mode operation, the inverted channel extends across the MOSFET, between the source and the drain (Fig. (b)). This conducting inversion layer on the surface effectively shields the substrate from the gate electric field; thus, Cgb = 0. In this case, the distributed gate-to-channel capacitance may be viewed as being shared equally between the source and the drain, yielding

$$C_{gs} \cong C_{gd} \cong \frac{1}{2} \cdot C_{ox} \cdot W \cdot L$$

(b)



When the MOSFET is operating in saturation mode, the inversion layer on the surface does not extend to the drain, but it is pinched off (Fig. (c)). The gate-to-drain capacitance component is therefore equal to zero (Cgd = 0) . Since the source is still linked to the conducting channel, its shielding effect also forces the gate-to-substrate capacitance to be zero, Cgb = 0. Finally, the distributed gate-to-channel capacitance as seen between the gate and the source can be approximated by

$$C_{gs} \cong \frac{2}{3} \cdot C_{ox} \cdot W \cdot L$$

(c)

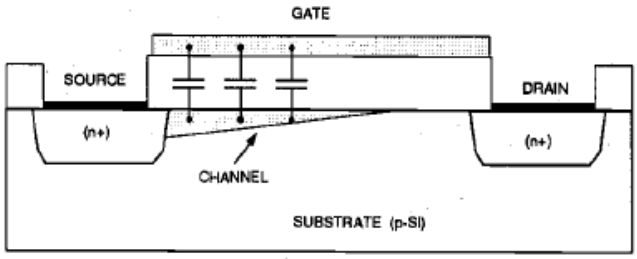


Figure.. Schematic representation of MOSFET oxide capacitances during (a)cut-off,(b)linear, and (c) saturation modes.

Capacitance	Cut-off	Linear	Saturation
C_{gb} (total)	$C_{ox}WL$	0	0
C_{gd} (total)	$C_{ox}WL_D$	$\frac{1}{2}C_{ox}WL + C_{ox}WL_D$	$C_{ox}WL_D$
C_{gs} (total)	$C_{ox}WL_D$	$\frac{1}{2}C_{ox}WL + C_{ox}WL_D$	$\frac{2}{3}C_{ox}WL + C_{ox}WL_D$

Table for Approximate oxide capacitance values for three operating modes of the MOS

Modeling of MOS Transistors including Basic concept the SPICE level-1 models,the level -2 and level-3 model

The LEVEL1 Model Equations

The LEVEL 1 model is the simplest current-voltage description of the MOSFET, which is basically the GCA-based quadratic model originally proposed by Shichman and Hodges. The equations used for the LEVEL 1 n-channel MOSFET model in SPICE are as follows.

Linear Region

$$I_D = \frac{k'}{2}\cdot\frac{W}{L_{eff}}\cdot\left[2\cdot(V_{GS}-V_T)V_{DS}-V_{DS}^2\right]\cdot(1+\lambda V_{DS}) \quad \text{for} \quad V_{GS}\geq V_T$$

$$\text{and} \quad V_{DS} < V_{GS}-V_T \qquad \text{.....(1)}$$

Saturation Region

$$I_D = \frac{k'}{2}\cdot\frac{W}{L_{eff}}\cdot(V_{GS}-V_T)^2\cdot(1+\lambda\cdot V_{DS}) \qquad \text{for} \quad V_{GS}\geq V_T$$

$$\text{and} \quad V_{DS}\geq V_{GS}-V_T$$

Where the threshold voltage V_T is calculated as

$$V_T = V_{T0}+\gamma\cdot\left(\sqrt{|2\phi_F|+V_{SB}}-\sqrt{|2\phi_F|}\right)$$

Note that the effective channel length Le used in the equations is found as follows:

$$L_{eff} = L-2\cdot L_D$$

The LEVEL2 Model Equations

To obtain a more accurate model for the drain current, it is necessary to eliminate some of the simplifying assumptions made in the original GCA analysis.Specifically, the bulk depletion charge must be calculated by taking into account its dependence on the channel voltage. Solving the drain current equation using the voltage-dependent bulk charge term,the following current-voltage characteristics can be obtained:

$$I_D = \frac{k'}{(1-\lambda\cdot V_{DS})}\cdot\frac{W}{L_{eff}}\cdot\left\{\left(V_{GS}-V_{FB}-|2\phi_F|-\frac{V_{DS}}{2}\right)\cdot V_{DS} - \frac{2}{3}\cdot\gamma\cdot\left[(V_{DS}-V_{BS}+|2\phi_F|)^{3/2}-(-V_{BS}+|2\phi_F|)^{3/2}\right]\right\}$$

The saturation voltage V_{DSAT} can be calculated as

$$V_{DSAT} = V_{GS} - V_{FB} - |2\phi_F| + \gamma^2 \cdot \left(1 - \sqrt{1 + \frac{2}{\gamma^2} \cdot (V_{GS} - V_{FB})}\right)$$

The saturation mode current is

$$I_D = I_{Dsat} \cdot \frac{1}{(1 - \lambda \cdot V_{DS})}$$

The LEVEL3 Model Equations

The LEVEL3 model has been developed for simulation of short-channel MOS 'transistors;it can represent the characteristics of MOSFETs quite precisely for channel lengths down to 2 gum. The current-voltage equations are formulated in the same way as for the LEVEL2 model.

$$I_D = \mu_s \cdot C_{ox} \cdot \frac{W}{L_{eff}} \cdot \left(V_{GS} - V_T - \frac{1 + F_B}{2} \cdot V_{DS}\right) \cdot V_{DS}$$

Where

$$F_B = \frac{\gamma \cdot F_s}{4 \cdot \sqrt{|2\phi_F| + V_{SB}}} + F_n$$

The empirical parameter FB expresses the dependence of the bulk depletion charge on th
e three-dimensional geometry of the MOSFET .Here,the parameters VT, Fs, and us are influenced by the short-channel effects, while the parameter Fn is influenced by the narrow-channel effects. The dependence of the surface mobility on the gate electric field is simulatedas follows:

$$\mu_s = \frac{\mu}{1 + \theta \cdot (V_{GS} - V_T)}$$

Design Hierarchy, Design Styles &CAD Technology.

Design Hierarchy

The use of the hierarchy, or "divide and conquer" technique involves dividing a module into sub-modules and then repeating this operation on the sub-modules until the complexity of the smaller parts becomes manageable. This approach is very similar to software development wherein large programs are split into smaller and smaller sections until simple subroutines, with well-defined functions and interfaces, can be written. In the physical domain, partitioning a complex system into its various functional blocks will provide a valuable guide for the actual realization of these blocks on the chip.

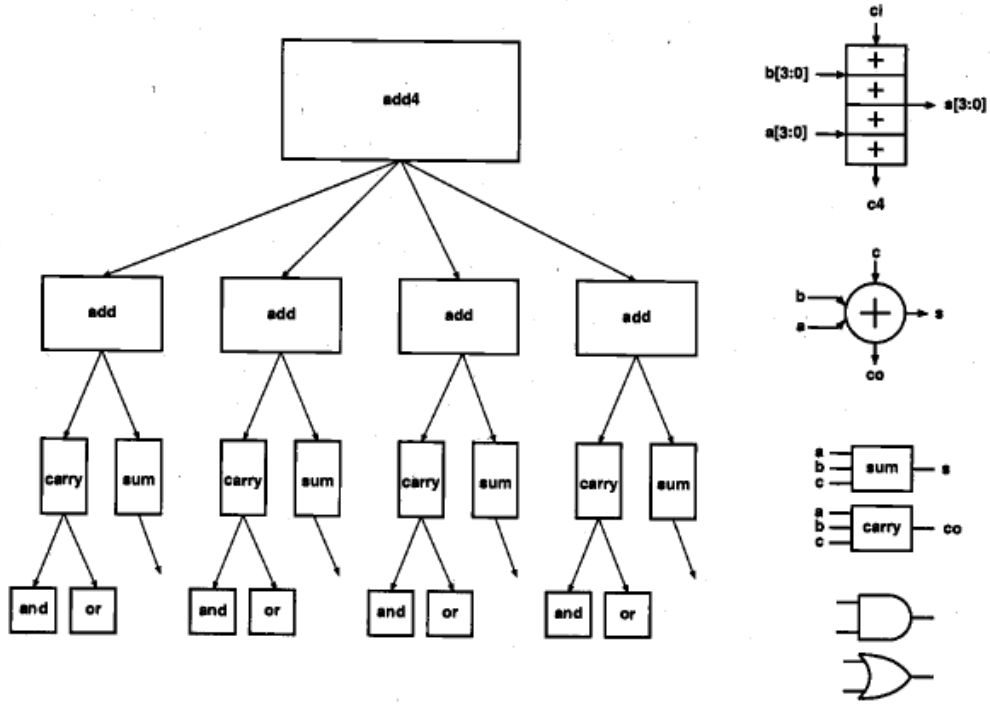


FIG-5(Structural decomposition of a4-bit adder,showing the levels of hierarchy).

Regularity,Modularity and Locality

Regularity means that the hierarchical decomposition of a large system should result in not only simple, but also similar blocks, as much as possible. A good example of regularity is the design of array structures consisting of identical cells – such as a parallel multiplication array.

Modularityindesignmeansthatthevariousfunctionalblockswhichmakeupthelargersystemmusthave*well-defined functions* and*interfaces.* Modularity allows hateach

block or module can be designed relatively independently from each other, since there is no ambiguity about the function and the signal interface of these blocks.

Locality also ensures that connections are mostly between neighboring modules,avoiding long-distance connections as much as possible.This last point is extremely important for avoiding long interconnect delays

Computer-Aided Design Technology

Computer-aided design(CAD)tools are essential for timely development of integrated circuits. Although CAD tools cannot replace the creative and inventive parts of the design activities, the majority of time-consuming and computation intensive mechanistic parts of the design can be executed by using CAD tools. The CAD technology for VLSI chip design can be categorized into the following areas:

* High level synthesis
* Logic synthesis
* Circuit optimization
* Layout
* Simulation
* Design rules checking

SynthesisTools

The high-level synthesis tools using hardware description languages (HDLs), such as VHDL or Verilog, address the automation of the design phase in the top level of the design hierarchy.

***Layout** Tools*

The tools for circuit optimization are concerned with transistorsizing forminimization of delays and with process variations, noise, and reliability hazards. The layout CAD tools include floor planning, place-and-route and module generation. Sophisticated layout tools are goal driven and includes ome degree of optimization functions.

Simulation and Verification Tools

The simulation category, which is the most mature area of VLSI CAD, includes many tools ranging from circuit-level simulation (SPICE orits derivatives, such as HSPICE),timing level simulation, logic level simulation, and behavioral simulation. Many ot her simulation tools have also been developed for device-level simulation and process simulation for technology development. The aim of all simulation CAD tools is to determine if the designed circuit meets the required specifications, at all stages of the design process.

Unit- 2
FABRICATION OF MOSFETS

Explain Fabrication processes (NMOS Fabrication, CMOS n-well process)FABRICATION PROCESS

The process starts with the creation of the n-well regions for p MOS transistors, by impurity implantation into the substrate. Then, a thick oxide is grown in the regions surrounding the n MOS and p MOS active regions. The thin gate oxide is subsequently grown on the surface through thermal oxidation. These steps are followed by the creation of n+ and p+ regions (source, drain, and channel stop implants) and by final metallization (creation of metal interconnects).

Each processing step requires that certain areas are defined on chip by appropriate masks. As a result patterned layers of doped silicon, polysilicon, metal, and insulating silicon dioxide. In general, a layer must be patterned before the next layer of material is applied on the chip. The process used to transfer a pattern to a layer on the chip is called *lithography.* Since each layer has its own distinct patterning requirements, the lithographic sequence must be repeated for every layer, using a different mask.

starts with the thermal oxidation of the silicon surface, by which an oxide layer of about 1 m thickness, for example, is created on the substrate (Fig. (b)). The entire oxide surface is then covered with a layer of photo-resist, which is essentially a light-sensitive, acid-resistant organic polymer, initially insoluble in the developing solution

If the photo-resist material is exposed to ultraviolet (UV) light, the exposed areas become soluble so that they are no longer resistant to etching solvents. To selectively expose the photo-resist, we have to cover some of the areas on the surface with a mask during exposure. Thus, when the structure with the mask on top is exposed to UV light, areas which are covered by the opaque features on the mask are shielded. In the areas where the UV light can pass through, on the other hand, the photo-resist is exposed and becomes soluble (Fig.(d)).

Thetypeofphoto-resistwhichisinitiallyinsolubleandbecomessolubleafterexposureto UV light is called*positive photo-resist.*

There is another type of photo-resist which is initially soluble and becomes insoluble(hardened) after exposure to UV light, called negative photo-resist. If negative photo-resist is used in the photo lithography process,

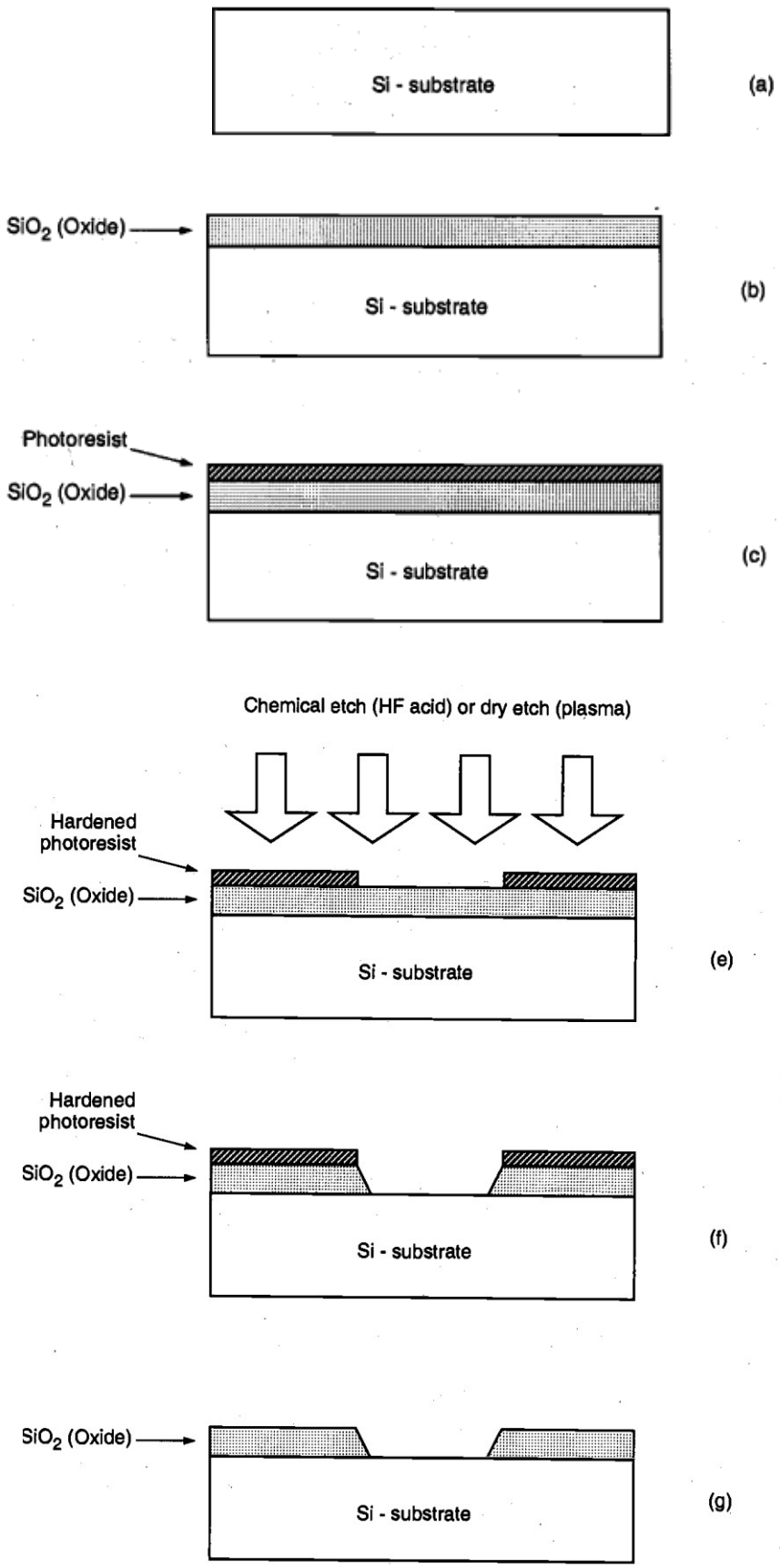


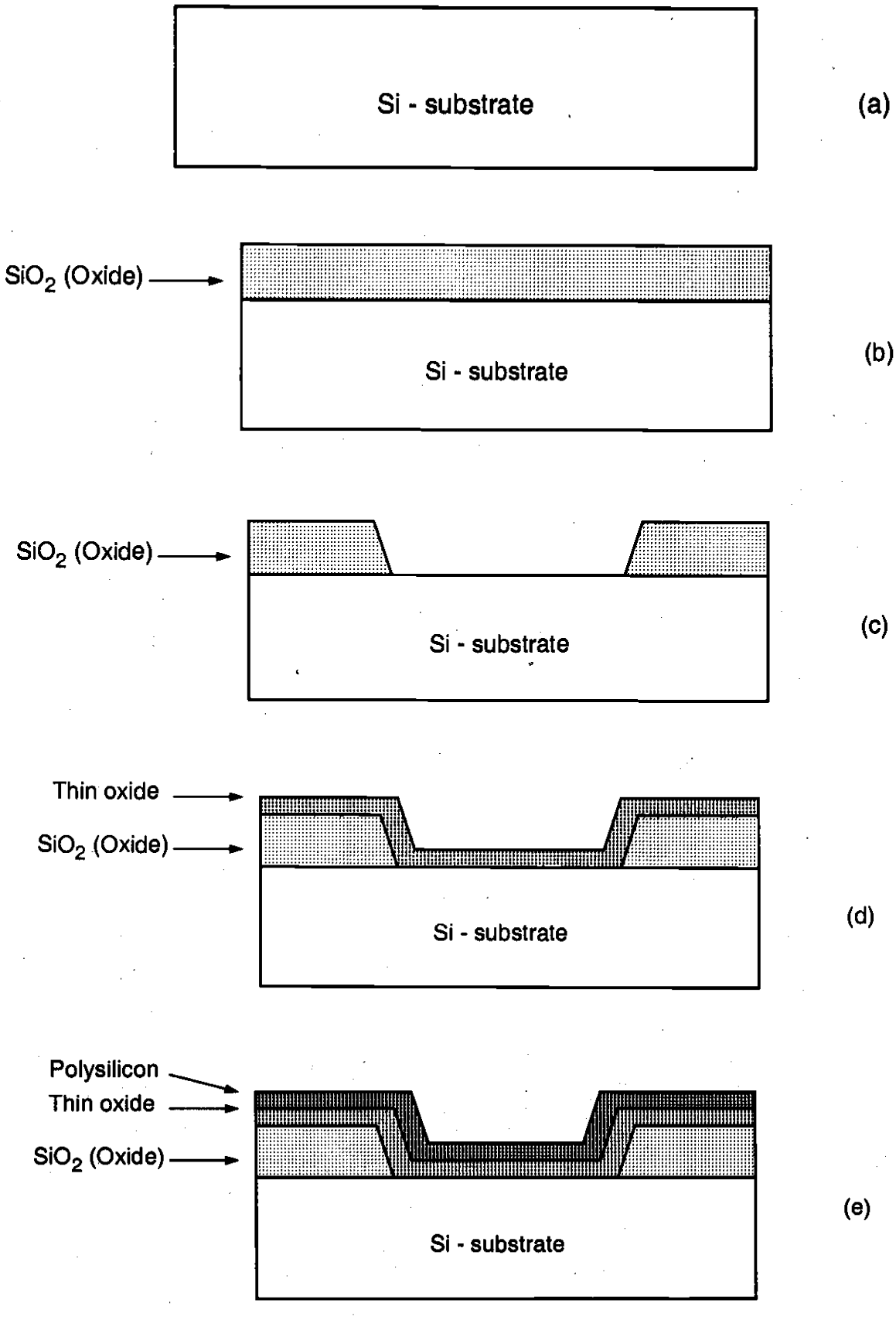
FIG-Processsteps required for patterning of silicon dioxide.

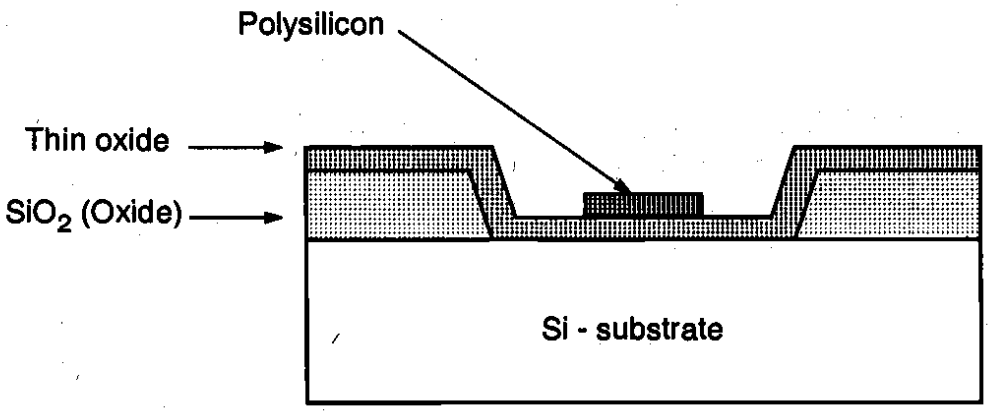
The areas which are not shielded from the UV light by the opaque mask features become insoluble, where as the shielded areas can subsequently be etched away by a developing solution. Negative photo-resists are more sensitive to light, but their photo lithographic resolution is not as high as that of the positive photo-resists. Therefore, negative photo-resistsare-used less commonly in the manufacturing of high-density integrated circuits.

Fabrication the N mos Transistor

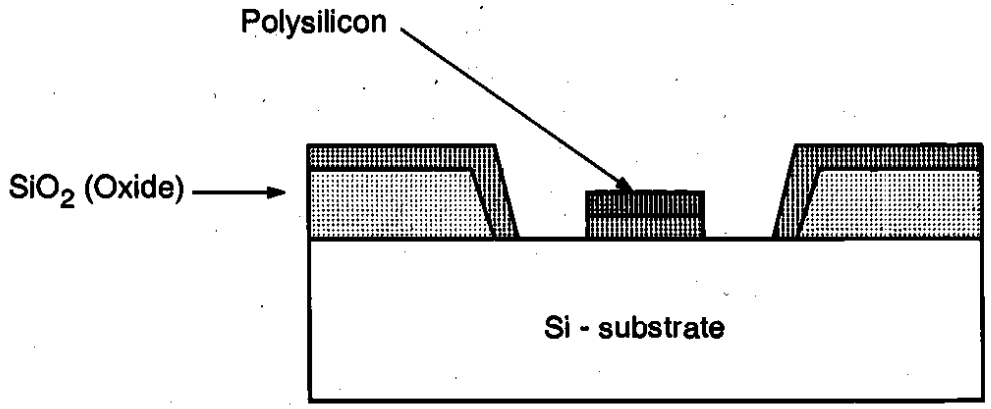
The process starts with of silicon substrate Fig in which a relatively thick dioxide layer, also called field oxide, is created on the surface Fig. Then, the field oxide is selectively etched to expose the silicon surface on which the MOS transistor will be created (Fig. (c)). Following this step, the surface is covered with a thin, high-quality oxide layer, which will eventually form the gate oxide of the n- mos transistor On top of the thin oxide layer, a layer of polysilicon (polycrystalline silicon) is deposited (Fig. (e)). Polysilicon is used both as gate electrode material for MOS transistors and also as an interconnect medium in silicon integrated circuits. Undoped polysilicon has relatively high resistivity. The-resistivity of polysilicon can be reduced, however, by doping it with impurity atoms.

After deposition , the poly silicon layer is patterned and etched to form the interconnects and the MOS transistor gates (Fig. (f)). The thin gate oxide not covered by polysilicon is also etched away, which exposes the bare silicon surface on which the source and drain junctions are to be formed (Fig. (g)). The entire silicon surface is then doped with ahigh concentration of impurities, either through diffusion or ion implantation (in this case with donor atoms to produce n-type doping). Figure (h) shows that the doping penetrates the exposed areas on the silicon surface, ultimately creating two n type regions (source and drain junctions) in the p-type substrate. The impurity doping also penetrates the polysilicon on the surface, reducing its resistivity. Note that the polysilicon gate, which is patterned *before* doping, actually defines the precise location of the channel region and, hence, the location of the source and the drain regions. Since this procedure allows very precise positioning of the two regions relative to the gate, it is also called the*self-aligned process.*



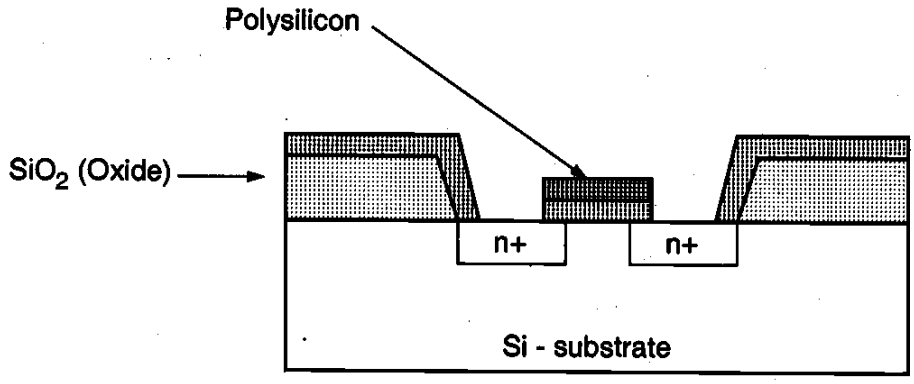


(f)

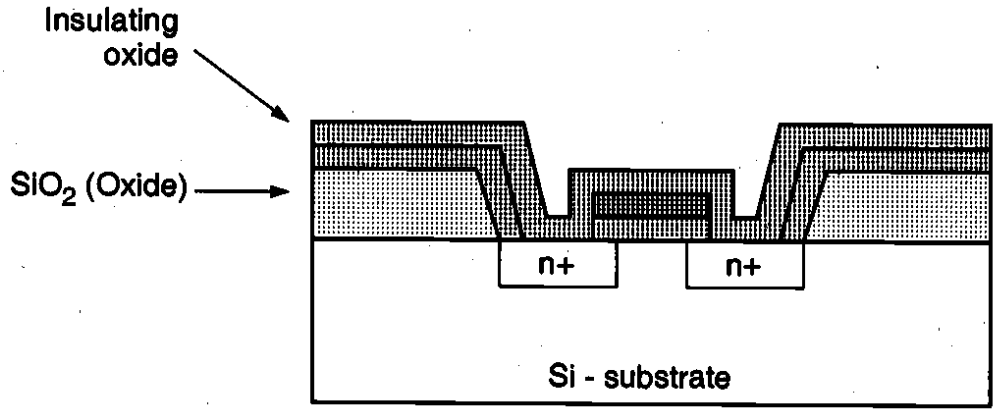


(g)

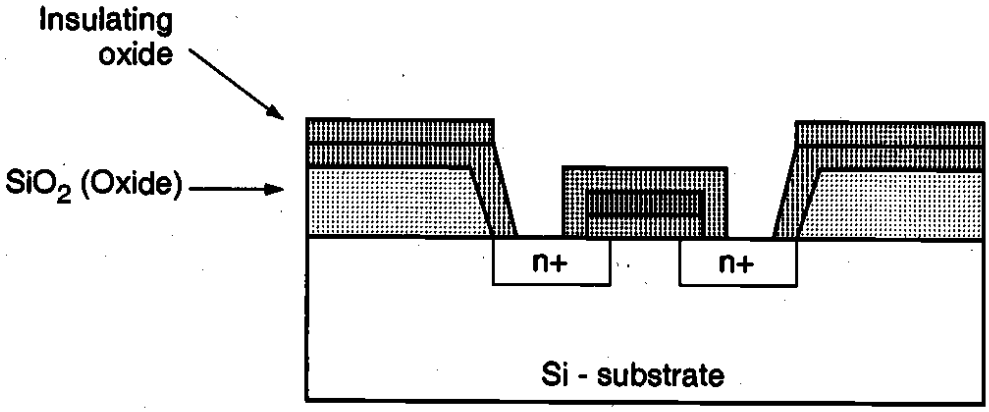
Once the source and drain regions are completed, the entire surface is again covered with an insulating layer of silicon dioxide(Fig.(i)).The insulating oxide layer is the n patterned in order to provide contact windows for the drain and source junctions (Fig.).The surface is covered with evaporated aluminum which will form the interconnects (Fig.). Finally, the metal layer is patterned and etched, completing the interconnection of the MOS transistors on the surface (Fig.). Usually, a second (and third) layer of metallic interconnect can also be added on top of this structure by creating another insulating oxide layer, cutting contact (via) holes, depositing, and patterning the metal. The major process steps for the fabrication of an n MOS transistor on p-type silicon substrate are also illustrated in Plate1 and Plate2.



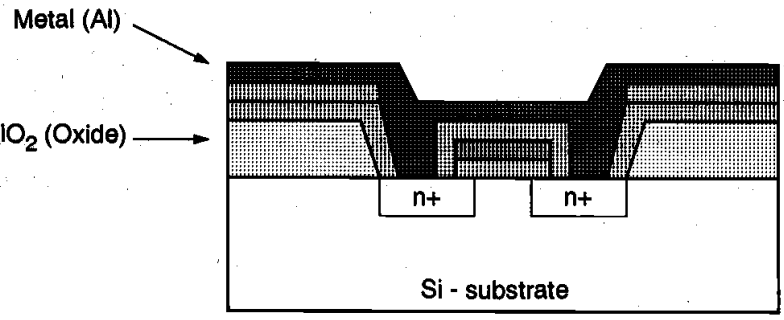
(h)



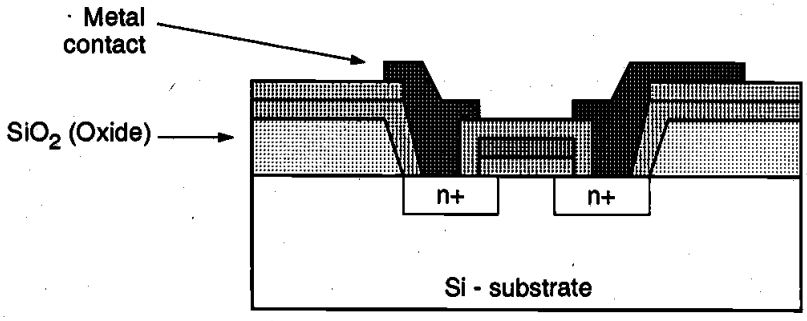
(i)



(j)



(k)



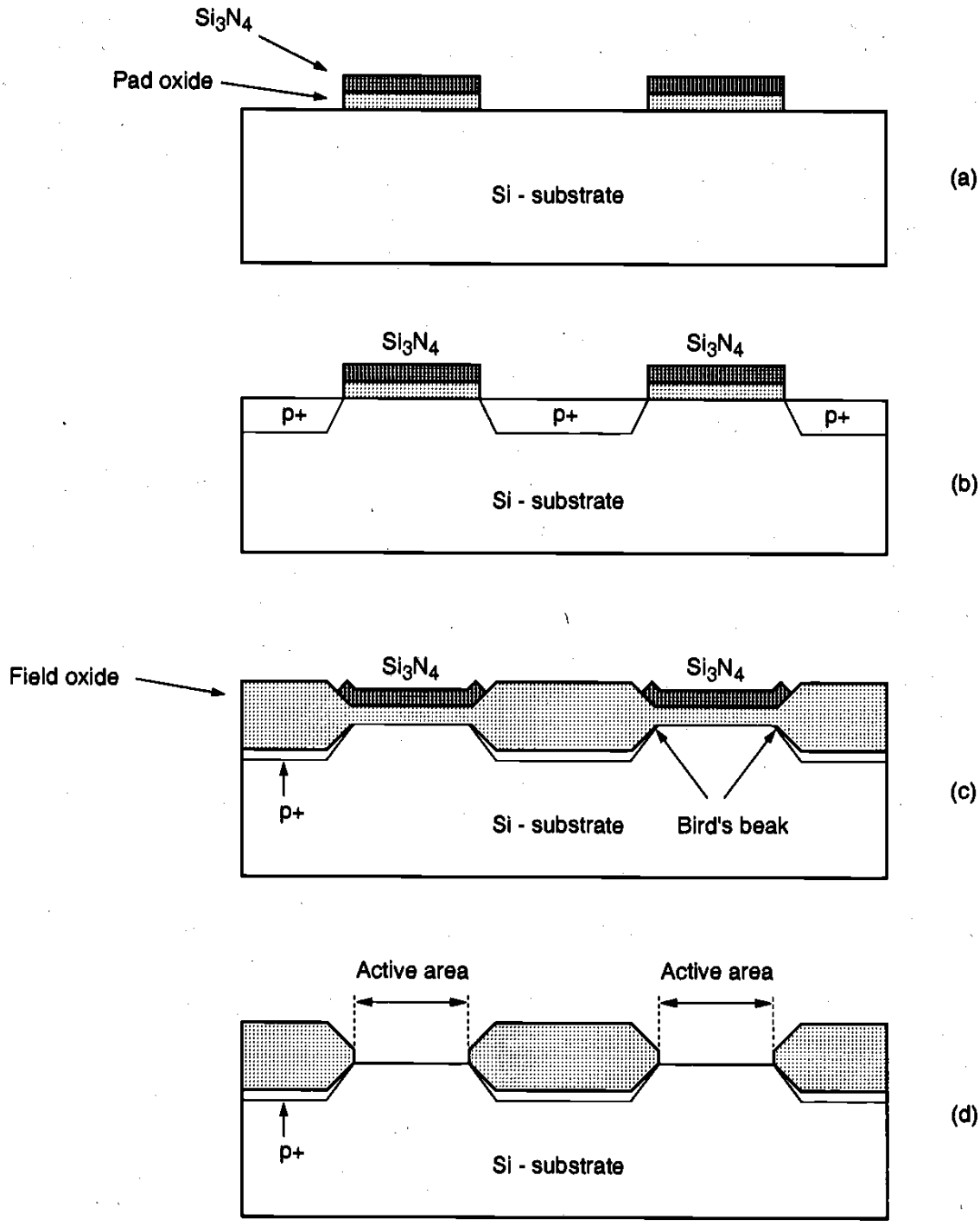
(l)

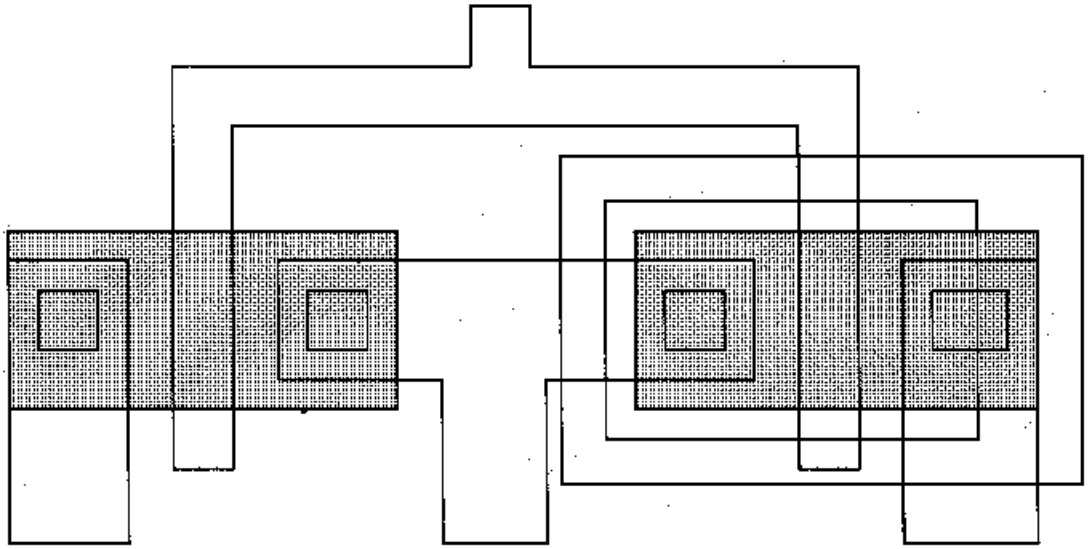
. Process flow for the fabrication of an n-type MOS transistor

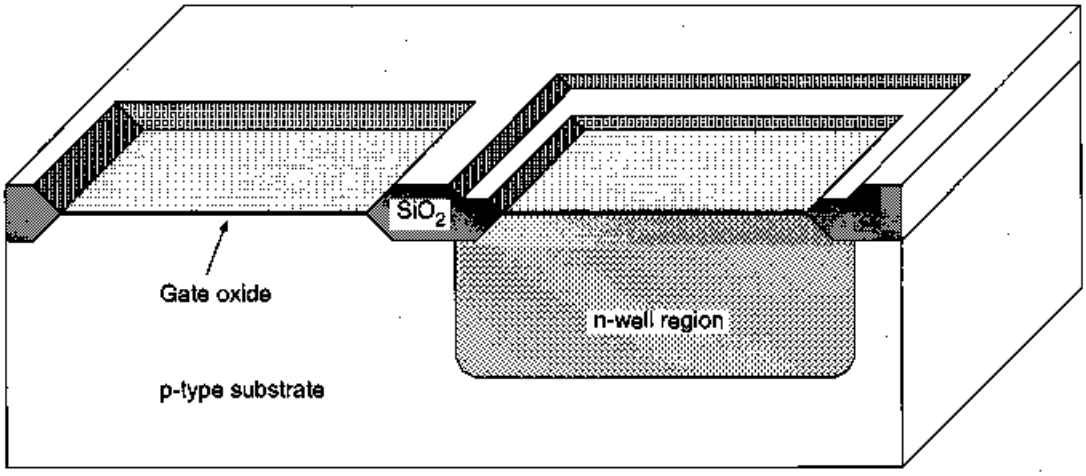
The CMOS n-Well Process

Having examined the basic process steps for pattern transfer through lithography and having gone through the fabrication procedure of a single n-type MOS transistor, we can now return to the generalized fabrication sequence of n-well CMOS integrated circuits , as shown in Fig.. In the following figures, some of the important process steps involved in the fabrication of a CMOS inverter will be shown by a top view of the lithographic masks and across-sectional view of the relevant areas. The n-well CMOS process starts with a moderately doped (with impurity concentration typically less than 1015 cm-3) p-type silicon substrate. Then, an initial oxide layer is grown on the entire surface. The first lithographic mask defines the n-well region. Donor atoms, usually phosphorus, are implanted through this window in the oxide.

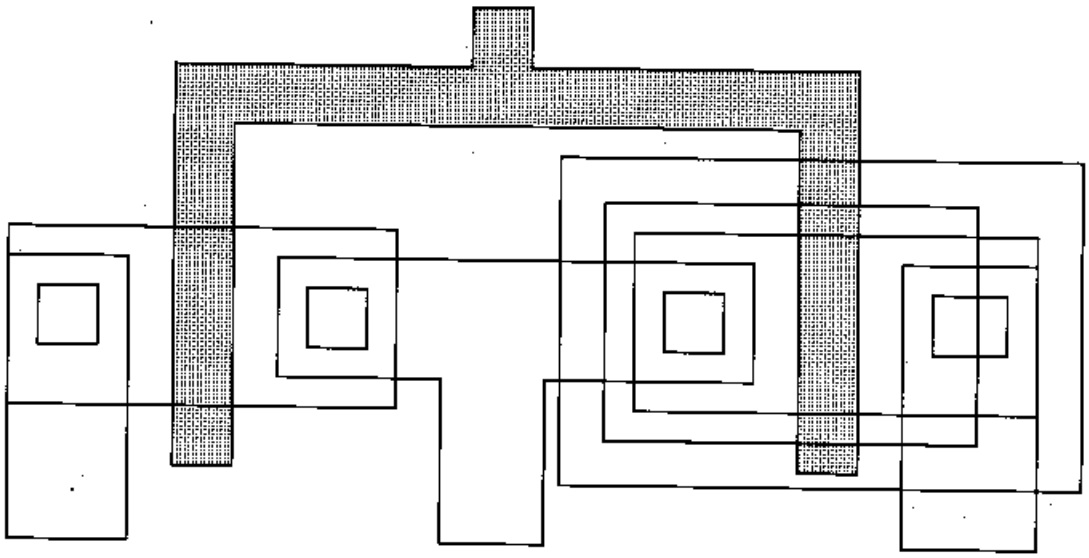
Once the n-well is created, the active areas of the n MOS and p MOS transistors can be defined. Figures through illustrate the significant milestones that occur during the fabrication process of a CMOS inverter. The main process steps for the fabrication of a CMOS inverter are also illustrated in Plate3, Plate4 and Plate5.

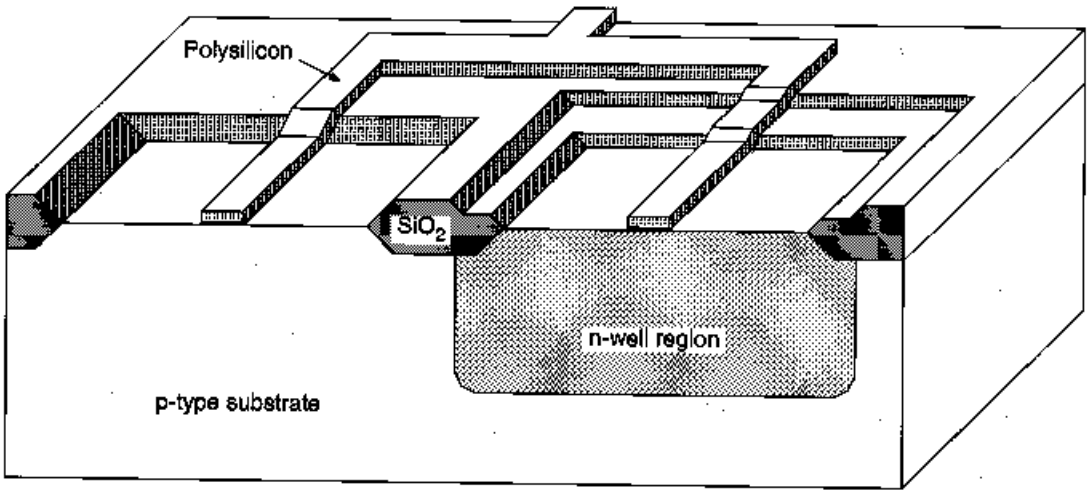




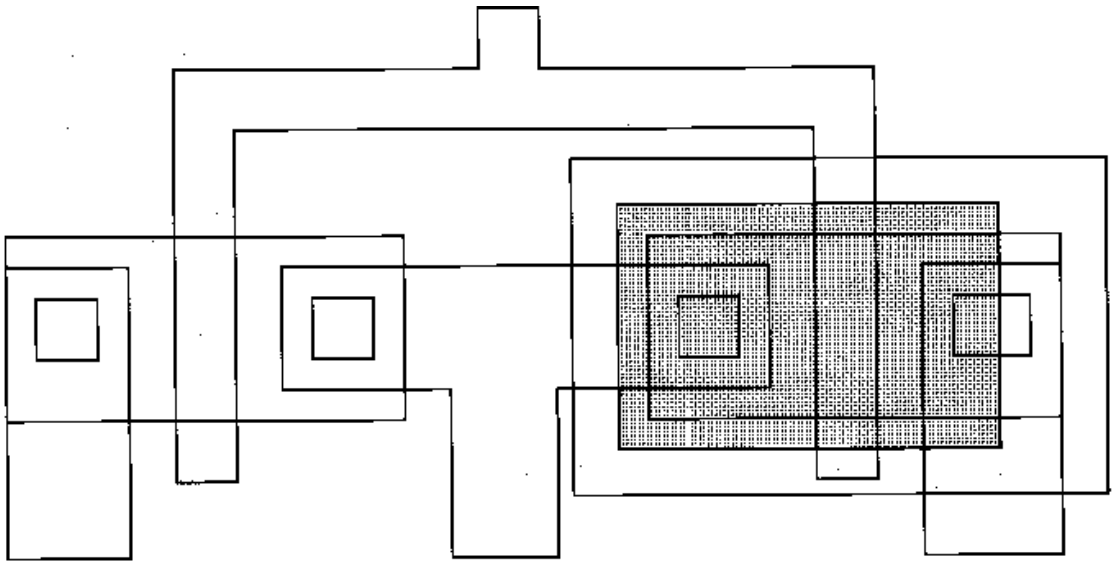


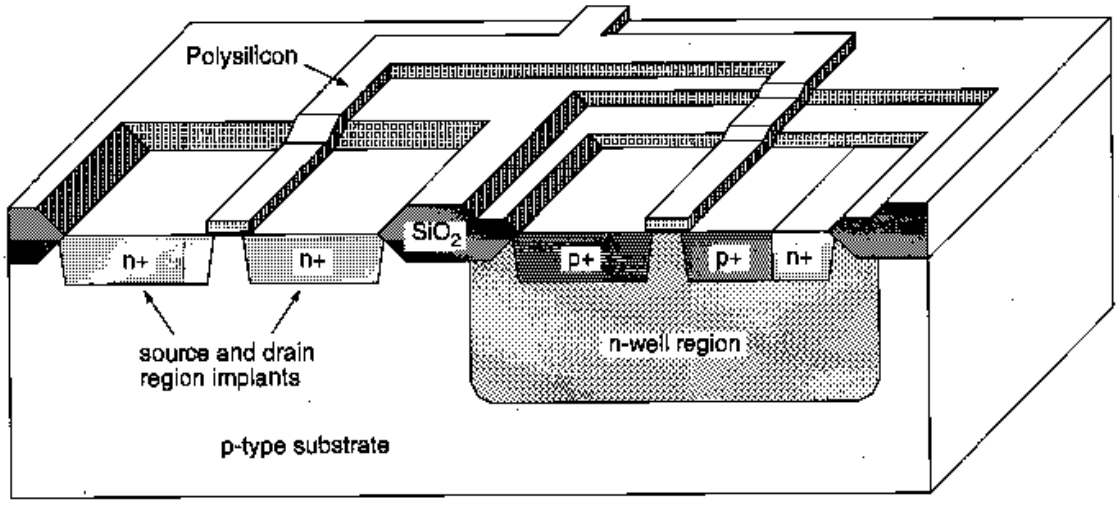
Following the creation of the n-well region, a thick field oxide is grown in the are as surrounding the transistor's active regions, and a thin gate oxide is grown on top of the active regions



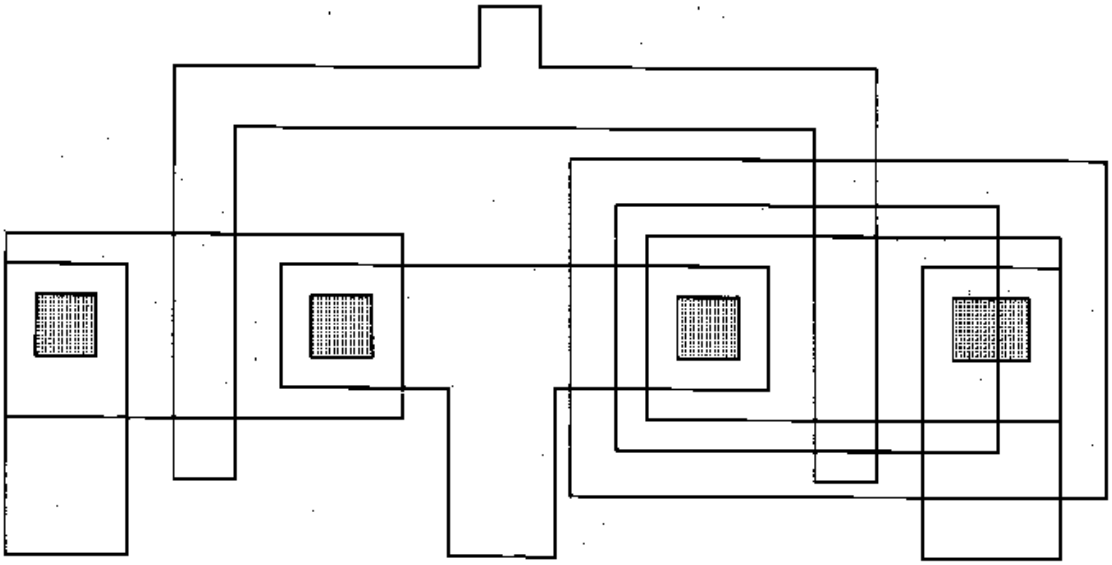


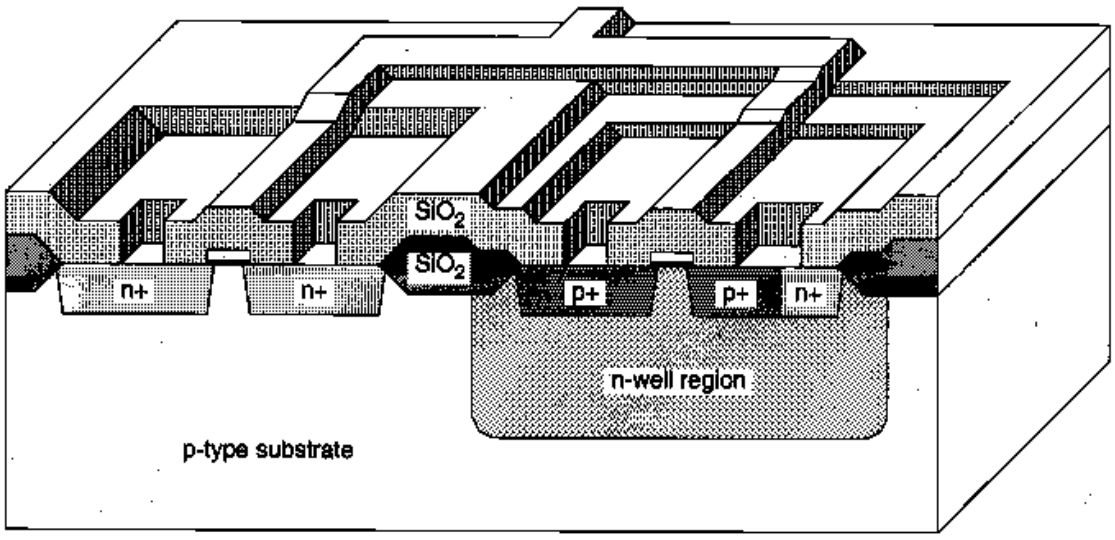
The poly silicon layer is deposited using chemical vapor deposition (CVD) and patterned by dry (plasma) etching. The created polysilicon lines will function as the gate electrodes of then MOS and the p MOS transistors and their interconnects.



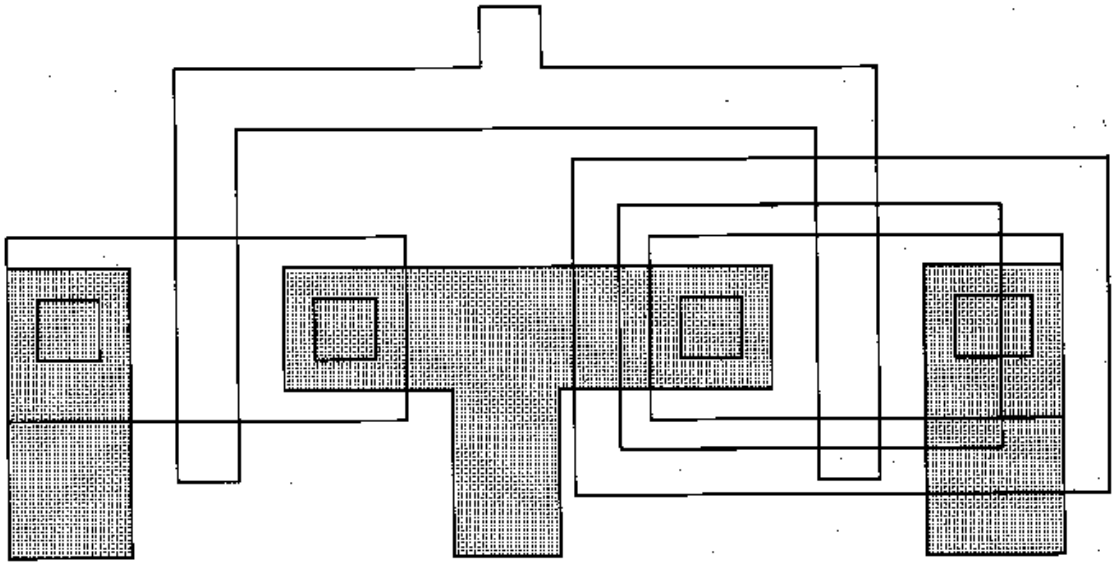


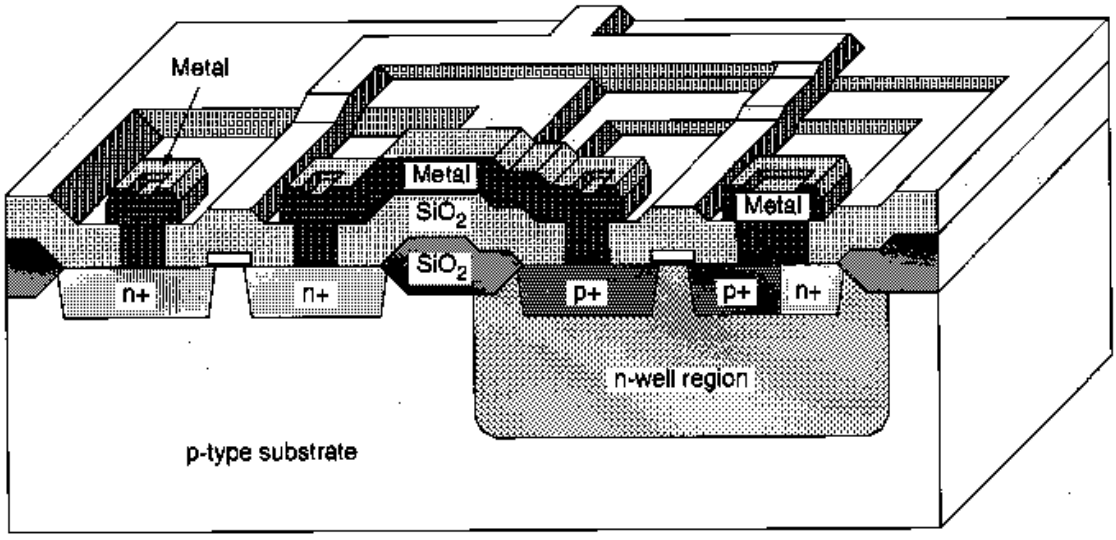
Using as of two masks, the n+ and p+ regions are implanted into the substrate and in to the n-well, respectively.



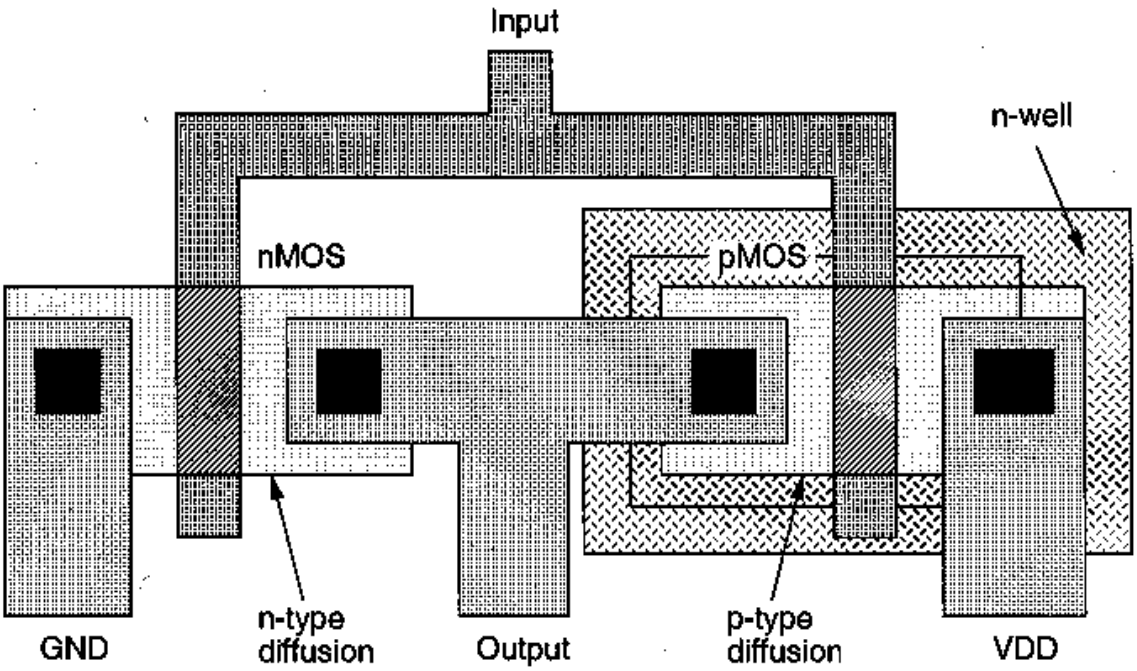


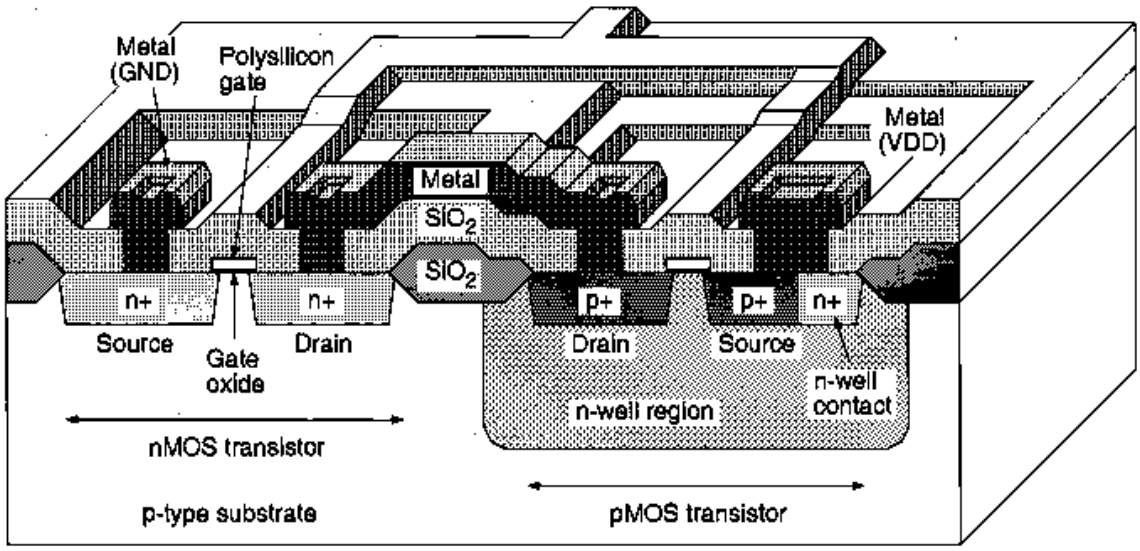
An insulating silicon dioxide layer is deposited over the entire wafer using CVD. Then, the contacts are defined and etched away to expose the silicon or polysilicon contact windows. These contact windows are necessary to complete the circuit interconnections using the metal layer,





Metal (aluminum) is deposited over the entire chip surface using metal evaporation, and the metal lines are patterned through etching. Since the wafer surface is non-planar, the quality and the integrity of the metal lines created in this step are very critical and are ultimately essential for circuit reliability.





The composite layout and the resulting cross-sectional view of the chip, showing onen MOS and one p MOS transistor (in then-well),and the poly-silicon and metal interconnections. The final step is to deposit the passivation layer (for protection) over the chip, except over wire-bonding pad areas

Explain Design rules

The physical mask layout of any circuit to be manufactured using a particular process must conform to a set of geometric constraints or rules, which are generally called layout design rules. These rules usually specify the minimum allowable line widths for physical objects on-chip such as metal and polysilicon interconnects or diffusion areas, minimum feature dimensions, and minimum allowable separations between two such features.

The design rules are usually described in two ways:

(i) Micron rules, in which the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of absolute dimensions in micro meters, or,

(ii) Lambda rules, which specify the layout constraints in terms of a single parameter () and thus allow linear, proportional scaling of all geometrical constraints.

Lambda-based layout design rules were originally devised to simplify the industry standard micron-based design rules and to allow scaling capability for various processes. It must be emphasized,

Active area rules

Minimum active area width 3λ

Minimum active area spacing 3 λ

Poly silicon rules

Minimum poly width 2 λ Minimum

poly spacing2λ

Minimum gate extension of poly over active 2

λ Minimum poly-active edge spacing L λ

(poly outside active area)

Minimumpoly-activeedgespacing3λ (poly

inside active area)

Metal rules

Minimum metal width 3 λ

Minimum metal spacing 3 λ

Contact rules

Poly contact size2 λ

Minimum polycontactspacing2λ

STICK DIAGRAM

It is the Stick and colour representation of the n- mos and c-mos circuit presentation and constructed as per the given rules

We have follow the rules as per the NAND and NOR gate constructions that is series connection in n- mos for NAND and parallel connection in p-mos similarly parallel connection for NOR gate in n- mos and series in p- mos

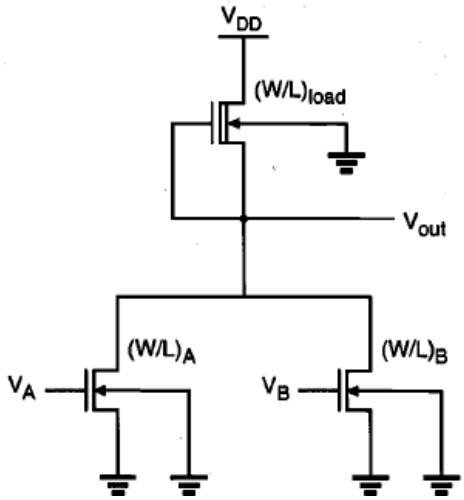


FIG.CIRCUIT DIAGRAM OF NOR GATE

Example-NORGATE

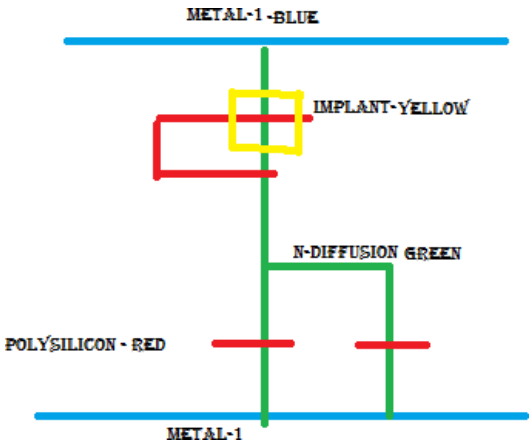


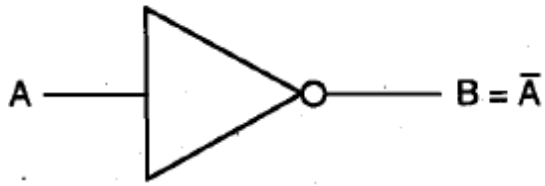
FIG. STICK DIAGRAM OF NOR GATE.

Similarly every other gate can constructed following these conditions.

Chapter 3
MOS Inverter

Basic NMOS inverters, characteristics,

The logic symbol and the truth table of the ideal inverter are shown in Fig.. In MOS inverter circuits, both the input variable A and the output variable B are represented by node voltages, referenced to the ground potential. Using positive logic convention, the Boolean (or logic) value of "1" can be represented by a high voltage of V_{DD}, and the Boolean(or logic) value of "0" can be represented by a low voltage of 0. The DC voltage transfer characteristic (V_{TC}) of the ideal inverter circuit is shown in Fig. 2. The voltage V_{th} is called the inverter threshold voltage. Note that for any input voltage between 0 and $V_{th}= V_{DD}/2$, the output voltage is equal to V_{DD}(logic"1).



Symbol

A	B
0	1
1	0

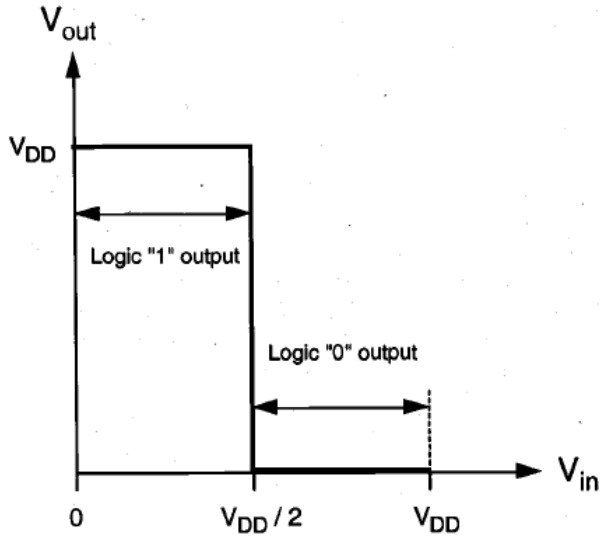
Truth Table

Logicsymbolandtruthtableoftheinverter

The output switches from V_{DD} to 0 when the input is equal to V_{th}. For any input voltage between V_{th} and V_{DD}, the output voltage assumes a value of 0 (logic "0"). Thus, an input voltage 0 < Vi. < V is interpreted by this ideal inverter as a logic "0," while an input voltage V_{th}<Vin < V_{DD}s interpreted as a logic " 1." The DC characteristics of actual inverter circuits will obviously differ in various degrees from the ideal characteristic shown in Fig.. The accurate estimation and the manipulation of the shape of V_{TC} for various inverter types are actually important parts of the design process.

Figure 3 shows the generalized circuit structure of an n MOS inverter. The input voltage of the inverter circuit is also the gate-to-source voltage of the n MOS transistor ($V_{in}=V_{Gs}$),while the output voltage of the circuit is equal to the drain-to- source voltage($V_{out}=V_{DS}$). The source and the substrate terminals of the n MOS transistor, also called the driver transistor, are connected to ground potential; hence,

the source-to-substrate voltage is V_{SB}= 0. In this generalized representation, the load device is represented as a two-terminal circuit element with terminal current IL and terminal voltage $V_L(I_L)$.



Voltage transfer characteristic(VTC) of the ideal inverter.

Voltage Transfer Characteristic (VTC)

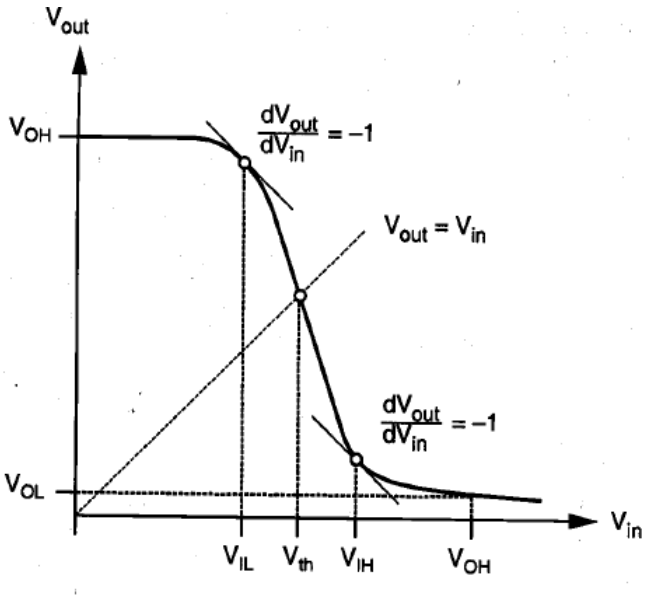
Applying Kirchhoff s Current Law (KCL) to this simple circuit, we see that the load current is always equal to the n MOS drain current.

$$I_D(V_{in}, V_{out}) = I_L(V_L) \quad \text{.....(1)}$$

Thevoltagetransfercharacteristicdescribing$V$asafunctionof$V$inunderDCconditions can then be found by analytically solving equation (1) for various input voltage values. The typical VTC of a realistic n MOS inverter is shown in Fig. Upon examination, we can identify a number of important properties of this DC transfer characteristic.

The general shape of the VTC in Fig. is qualitatively similar to that of the ideal inverter transfer characteristic shown in Fig. There are, however, several significant differences that deserve special attention. For very low input voltage levels, the output voltage V is equal to the high value of *VOH (output high voltage).* In this case, the driver n MOS transistor is in cut-off, and hence, does not conduct any current. Consequently, the voltage drop across the load device is very small in magnitude, and the output voltage level is high. As the input voltage V increases, the driver transistor starts conducting a certain drain current, and the output voltage eventually starts to decrease. Notice that this drop in the

output voltage level does not occur abruptly, such as the vertical drop as summed for the ideal inverter VTC, but rather gradually and with a finite slope.



Typical voltage transfer characteristic (VTC) of a realistic nMOS inverter. We identify two*critical voltage points* on this curve, where the slope of the Vt (Vin) characteristic becomes equal to −1,i.e.,

$$\frac{dV_{out}}{dV_{in}} = -1$$

VOH: Maximum output voltage when the output level is logic " 1"VOL Minimum output voltage when the output level is logic "0"VIL: Maximum input voltage which can be interpreted as logic "0"VIH: Minimum input voltage which can be interpreted as logic "1"

Describe inverters with resistive load and with n-type & MOSFET load Resistive-Load Inverter

The basic structure of the resistive-load inverter circuit is shown in Fig.As in the general inverter circuit as shown in Fig. 2, an enhancement-type n MOS transistor acts as the driver device. The load consists of a simple linear resistor, RL. The power supply voltage of this circuit is VDD. Since the following analysis concentrates on the static behavior of the circuit, the output load capacitance is not shown in this figure.

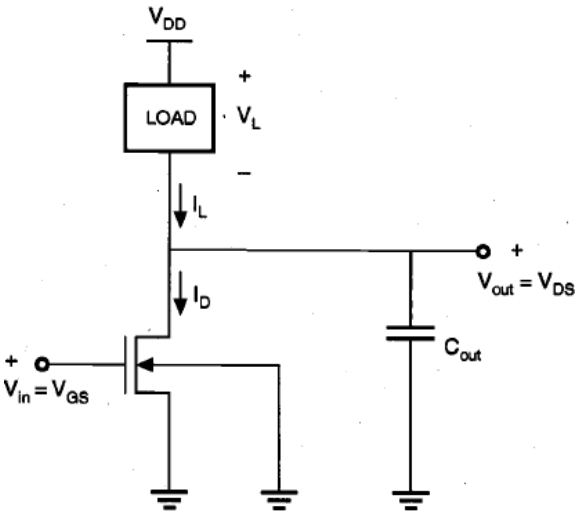


Fig.

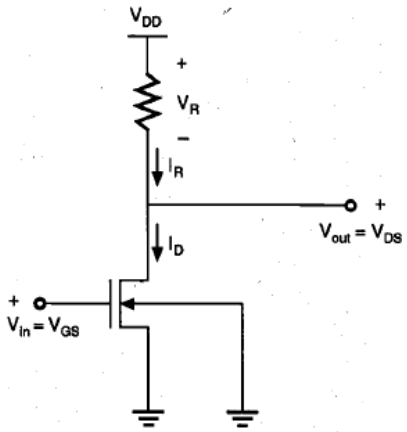


Fig.

As already noted in Section equation1, the drain current ID of the driver MOSFET is equal to the load current R in DC steady-state operation. To simplify the calculations, the channel-length modulation effect will be neglected in the following, i.e. ,A=0.Also,notethat the source and the substrate terminals of the driver transistor are both connected to theground;hence,VSB=0.Consequently,thethresholdvoltageofthedrivertransistorisalways equal to V.. We start our analysis by identifying the various operating regions of the driver transistor under steady-state conditions. For input voltages smaller than the threshold voltage V., the transistor is in cut-off, and does not conduct any drain current. Since the voltage drop across the load resistor is equal to zero, the output voltage must be equal to the power supply voltage, VDD. As the input voltage is increased beyond $V_{th.}$, the driver transistor starts conducting a nonzero drain current. Note that the driver

$$I_R = \frac{k_n}{2} \cdot (V_{in} - V_{T0})^2$$

MOSFET is initially in saturation, since its drain- to source voltage. (VDs=V_{out}) is larger than(V_{in}–$V_{GS.}$). Thus,

Inverters with n-Type MOSFET Load

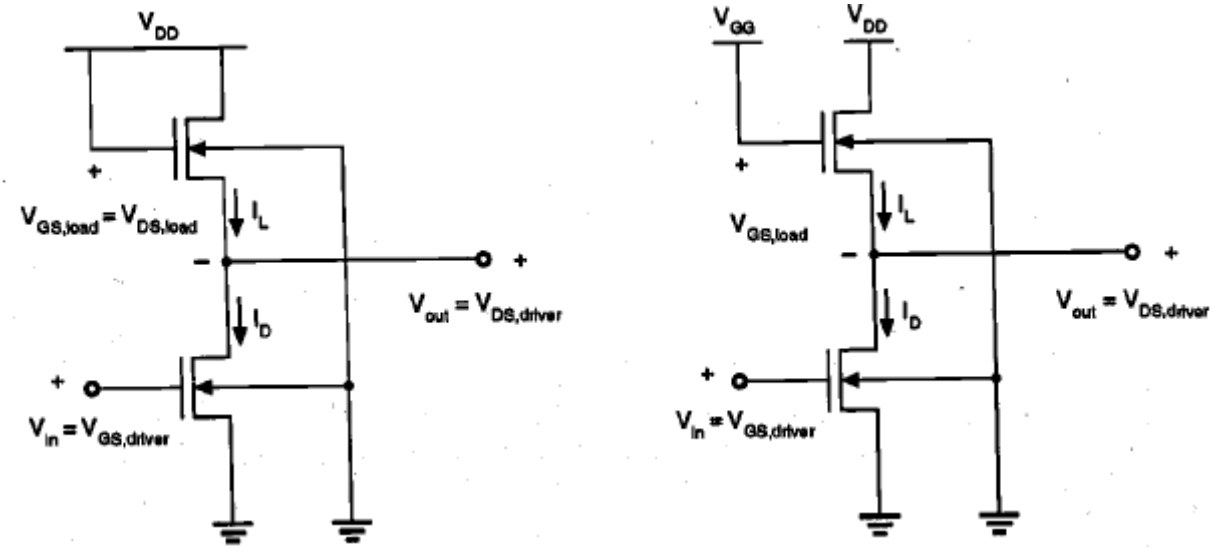
The simple resistive-load inverter circuit examined in the previous section is not a suitable candidate for most digital VLSI system applications, primarily because of the large area occupied by the load resistor. In this section, we will introduce inverter circuits, which use an n MOS transistor as the *active load* device, instead of the linear

load resistor. The main advantage of using a MOSFET as the load device is that the silicon are a occupied by the

transistor is usually smaller than that occupied by a comparable resistive load. More over, inverter circuit swith active loads can be designed to have better over all performance compared to that of passive-load inverters. In a chronological view, the development of inverters with an enhancement-type MOSFET load precedes other active-load inverter types, since its fabrication process was perfected earlier

Enhancement-Load n MOS Inverter

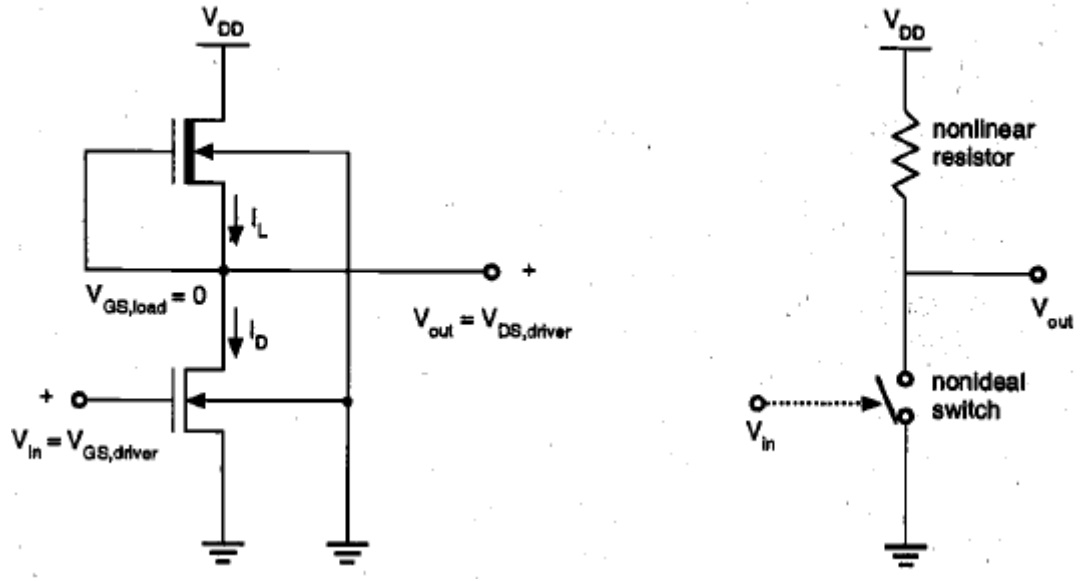
The circuit configurations of two inverters with enhancement-type load devices are shown in Fig. Depending on the bias voltage applied to its gate terminal, the load transistor can be operated either in the saturation region or in the linear region. Both types of inverters have some distinct advantages and disadvantages from the circuit design point of view.



Fig

Depletion-Load n MOS Inverter

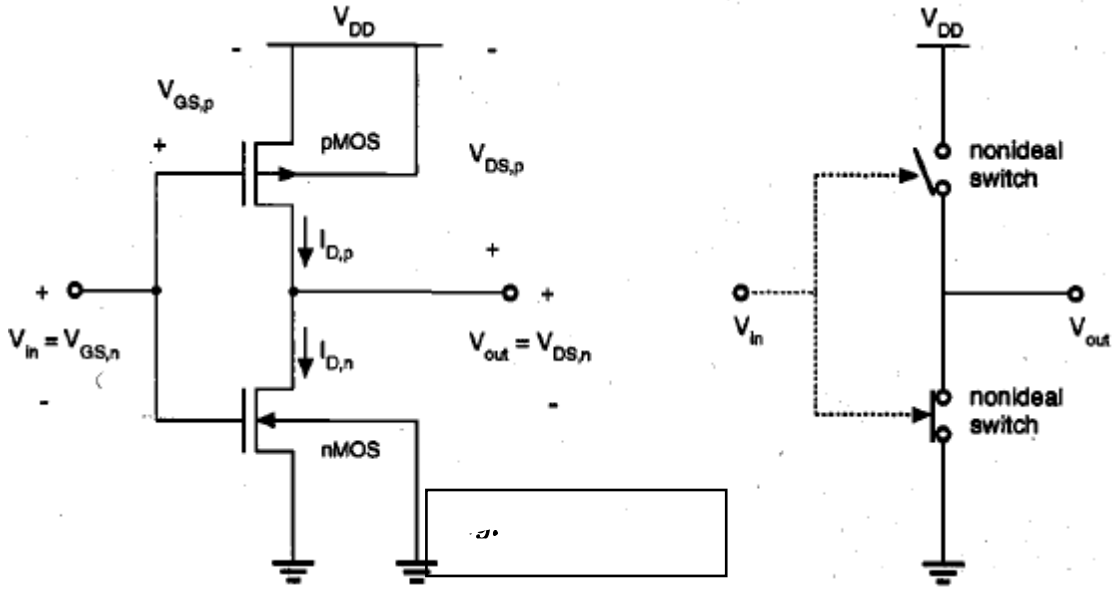
Several of the disadvantages of the enhancement-type load inverter can be avoided by using a depletion type n MOS transistor as the load device.- The fabrication process for producing an inverter with an enhancement-type n MOS driver and a depletion-type n MOS load is slightly more complicated and requires additional processing steps, especially for the channel implant to adjust the threshold voltage of the load device.



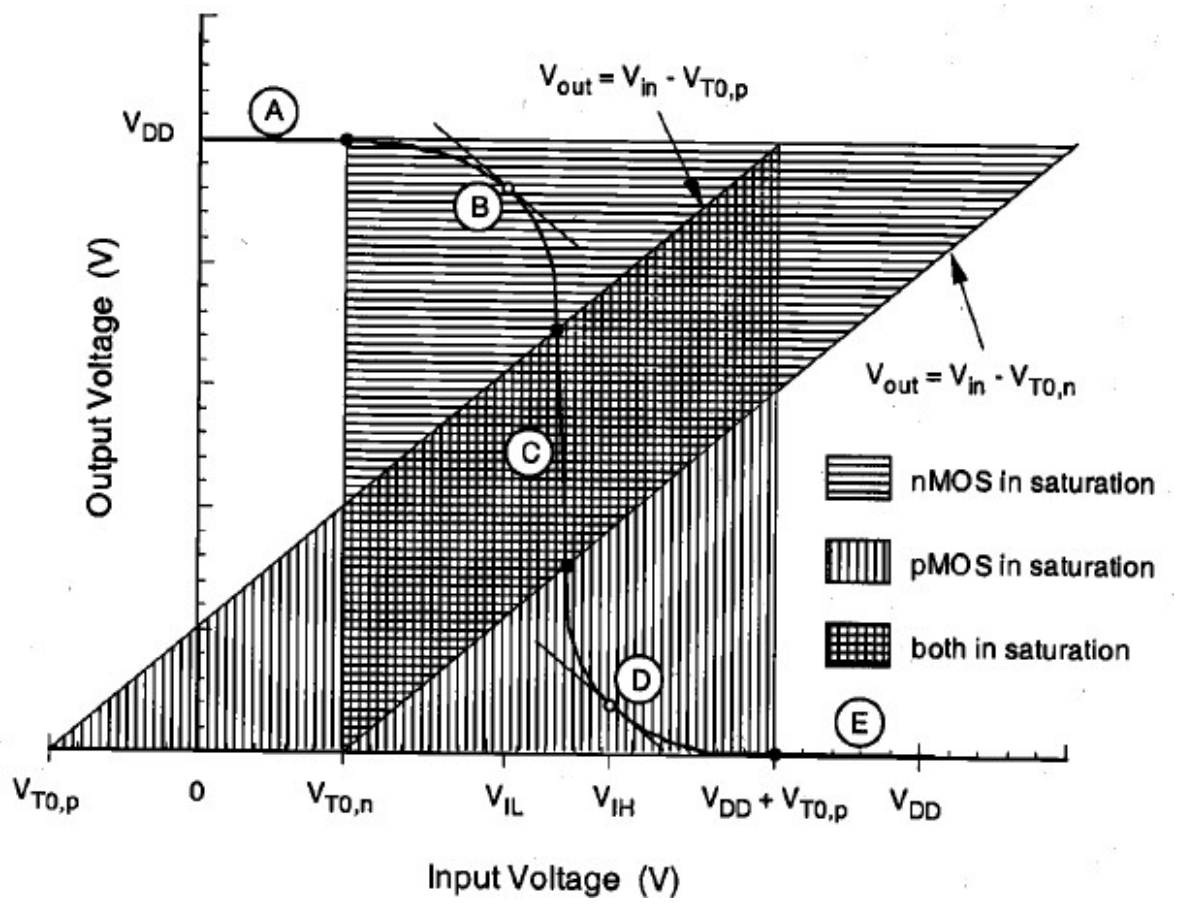
Fig

CMOS inverter and characteristics and interconnect effects : Delay time definitions

C-moswhichconsistsofanenhancement-typenMOStransistorandanenhancement-type p MOS transistor, operating in complementary mode (Fig.7 and 8). This configuration is called Complementary MOS(CMOS). The circuit topology is complementary push-pull in the sense that for high input, the n MOS transistor drives (pulls down) the output node while the p MOS transistor acts as the load, and for low input the p MOS transistor drives (pulls up) the output node while the n MOS transistor acts as the load. Consequently, both devices contribute equally to the circuit operation characteristics



(7) CMOS inverter circuit. (8)Simplified view of the CMOS inverter, consisting of two complementary nonideal switches.



Operating regions of then MOS and the p MOS transistors.

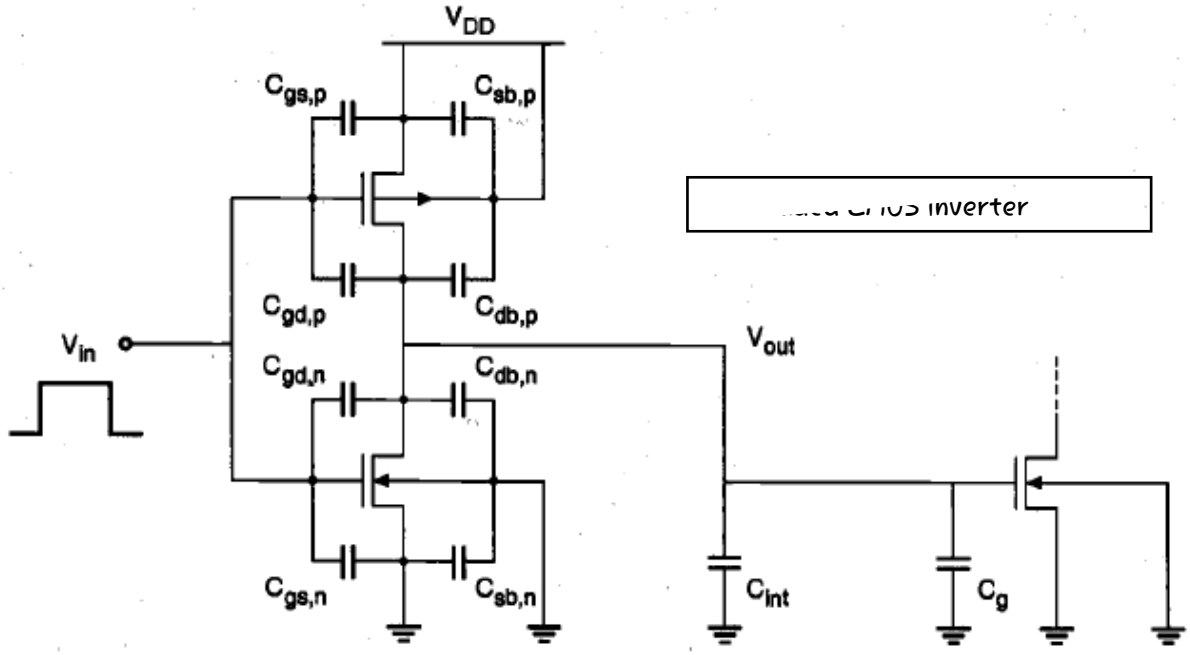
Both of these conditions for device saturation are illustrated graphically as shaded areas on the Vu -V plane in Fig. typical CMOS inverter voltage transfer characteristic is also superimposed for easy reference. Here , we identify five distinct regions, labeled A through E, each corresponding to a different set of operating conditions. The table below lists these regions and the corresponding critical input and output voltage levels.

Region	V_{in}	V_{out}	nMOS	pMOS
A	$< V_{T0,n}$	V_{OH}	cut-off	linear
B	V_{IL}	high $\approx V_{OH}$	saturation	linear
C	V_{th}	V_{th}	saturation	saturation
D	V_{IH}	low $\approx V_{OL}$	linear	saturation
E	$>\left(V_{DD} + V_{T0,p}\right)$	V_{OL}	linear	cut-off

Consider the cascade connection of two CMOS inverter circuits shown in Fig. .The parasitic capacitances associated with each MOSFET are illustrated individually. Here, the capacitances C_{gd} and C_{gs} are primarily due to gate overlap with diffusion, while C_{db} and C_{sb} are voltage-dependent junction capacitances, as discussed in Chapter 3. The 'capacitance component C_g is due to the thin-oxide capacitance over the gate area. In addition, we also consider the lumped interconnect capacitance C_{int}, which represents the parasitic capacitance contribution of the metal or polysilicon connection between the two inverters. It is assumed that a pulse waveform is applied to the input of the first-stage inverter.

The problem of analyzing the output voltage waveform is fairly complicated, even forth is relatively simple circuit, because a number of nonlinear, voltage-dependent capacitances are involved. To simplify the problem, we first combine the capacitances seen in Fig. into an equivalent *lumped* linear capacitance, connected between the output node of the inverter and the ground. This combined capacitance at the output node will be called the load capacitance, C_{load}

$$C_{load} = C_{gd,n} + C_{gd,p} + C_{db,n} + C_{db,p} + C_{int} + C_g$$



The propagation delay times τ_{PHL} and τ_{PLH} determine the input-to-output signal delay during the high to-low and low-to-high transitions of the output, respectively. By definition, τ_{PHL} is the time delay between the V50%-transition of the *rising* input voltage

and the V50-

Transition of *the falling* output voltage. Similarly, τ_{PLH} is defined as the time delay between the V50 -transition of *the falling* input voltage and the V50%-transition of the *rising* outputvoltage.

$$V_{50\%} = V_{OL} + \frac{1}{2}(V_{OH} - V_{OL}) = \frac{1}{2}(V_{OL} + V_{OH})$$

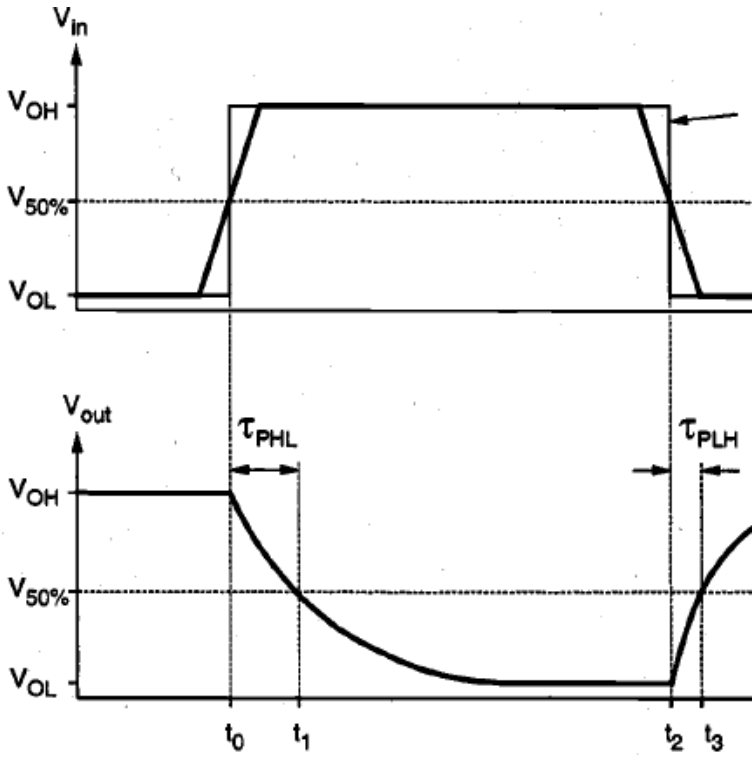
Thus, the propagation delay times τ_{PHL} and τ_{PLH} are found from Fig. as

$$\tau_{PHL} = t_1 - t_0$$

$$\tau_{PLH} = t_3 - t_2$$

The average propagation delay τ_P of the inverter characterizes the average time required for the input signal to propagate through the inverter.

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2}$$



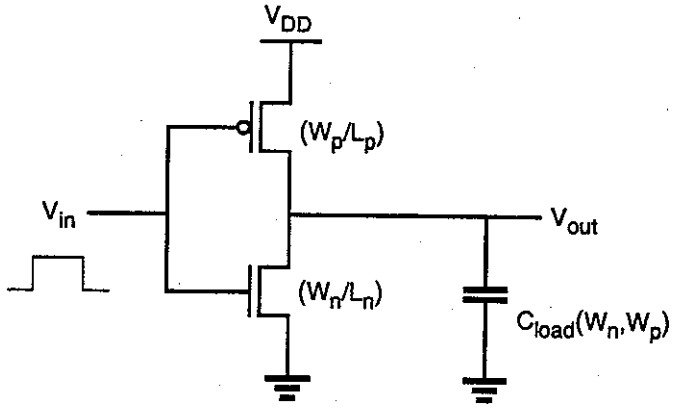
(Input and output voltage waveforms of a typical inverter, and the definitions of propagation delay times. The input voltage waveform is idealized as a step pulse for simpliciy.)

Invertor design with delay constraints.

The propagation delay equations on chart4-5 can be rearranged to solve for W/L, as shown below, where we substituted $C_{ox}\mu_n(W_n/L_n)$ fork_n and similarly fork_p

These equations can then be used to size a CMOS circuit to achieve a desired minimum rising or falling propagation delay assuming C_{load} and other parameters are known

After determining the desired W/L values, we can obtain the device widths W based on the technology minimum design device lengths L . Other constraints such as rise time/fall time or rise/fall symmetry may also need to be considered in addition to rise and fall delay.



$$\left(\frac{W_n}{L_n}\right)=\frac{C_{load}}{\tau^*_{PHL}\,\mu_n\,C_{ox}\left(V_{DD}-V_{T,n}\right)}\left[\frac{2\,V_{T,n}}{V_{DD}-V_{T,n}}+\ln\left(\frac{4\left(V_{DD}-V_{T,n}\right)}{V_{DD}}-1\right)\right]$$

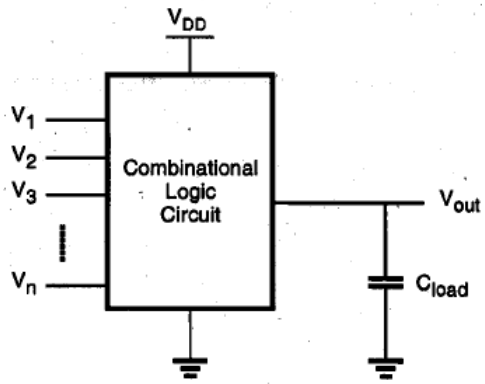
$$\left(\frac{W_p}{L_p}\right)=\frac{C_{load}}{\tau^*_{PLH}\,\mu_p\,C_{ox}\left(V_{DD}-\left|V_{T,p}\right|\right)}\left[\frac{2\left|V_{T,p}\right|}{V_{DD}-\left|V_{T,p}\right|}+\ln\left(\frac{4\left(V_{DD}-\left|V_{T,p}\right|\right)}{V_{DD}}-1\right)\right]$$

Unit- 4

Static, Combinational, Sequential& Dynamics logic circuits & Memories

MOS logic circuits & CMOS logic circuits. State style, complex logic circuits, pass transistor logic.

In its most general form, a combinational logic circuit, or gate, performing a Boolean function can be represented as a multiple-input single-output system, as depicted in Fig. .All input variables are represented by node voltages, referenced to the ground potential. Using *positive logic convention,* the Boolean (or logic) value of " 1 " can be represented by ahigh voltage of *VDD,* and the Boolean (or logic) value of "0" can be represented by a lowvoltageof0.Theoutputnodeisloadedwithacapacitance*CL,* whichrepresentsthecombinedparasiticdevicecapacitancesinthecircuitandtheinterconnectcapacitancecomponents *seen* by the output node. This output load capacitance certainly plays a very significant role in the dynamic operation of the logic gate.



MOS Logic Circuits with Depletion n MOS Loads

Two-Input NOR Gate

The first circuit to be examined in this section is the two-input NOR gate. The circuit diagram, the logic symbol, and the corresponding truth table of the gate are given in Fig. .The Boolean OR operation is performed by the parallel connection of the two enhancement-type n MOS driver transistors.