



MAHARAJA POLYTECHNIC, TARABAI, BHUBANESWAR.  
LESSON PLAN

NAME OF FACULTY: *Manisha Par Saral*  
BRANCH & SEMESTER:-ETC (5TH SEM)  
TOTAL NO. OF STUDENT IN THE CLASS:-06  
TOTAL NO. OF CLASSES REQUIRED:-60  
SESSION:-2021-22

SUBJECT NAME:- VLSI & EMBEDDED SYSTEM  
SUBJECT CODE:-TH-2

Sl. No.	Topics to be covered	Topics covered on date	Total no. of students present	Verified By HOD	Verified by the principal	Remark
	Unit-1: Introduction to VLSI & MOS Transistor					
1	Historical perspective- Introduction	9/11/21	6			
2	Classification of CMOS digital circuit types	9/11/21	6			
3	Introduction to MOS Transistor & Basic operation of MOSFET.	10/11/21	6			
4	Structure and operation of MOSFET (n-MOS enhancement type) & COMS	11/11/21	6			
5	MOSFET V-I characteristics	15/11/21	5			
6	Working of MOSFET capacitances	"				
7	Modelling of MOS Transistors including Basic concept the SPICE level-1 models, the level-2 and level-3 model.	16/11/21	6			
8	Flow Circuit design procedures	14/11/21	5			

9	VLSI Design Flow & Y chart	18/11/24	5	} <i>SPK</i>
10	Design Hierarchy			
11	VLSI design styles-FPGA, Gate Array Design, Standard cells based, Full custom Unit-2: Fabrication of MOSFET	22/11/24	5	
12	Simplified process sequence for fabrication	23/11/24	6	
13	Basic steps in Fabrication processes Flow	24/11/24	5	
14	Fabrication process of nMOS Transistor	29/11/24	5	
15	CMOS n-well Fabrication Process Flow	30/11/24	5	
16	MOS Fabrication process by n-well on p-substrate	2/12/24	6	
17	CMOS Fabrication process by P-well on n-substrate	6/12/24	6	
18	Layout Design rules	7/12/24	5	
19	Stick Diagrams of CMOS inverter Unit-3: MOS Inverter	'		
20	Basic nMOS inverters	8/12/24	6	} <i>SPK</i>
21	Working of Resistive-load Inverter	9/12/24	4	
22	Inverter with n-Type MOSFET Load – Enhancement Load, Depletion n-MOS inverter	13/12/24	6	
23	CMOS inverter – circuit operation and characteristics and interconnect effects: Delay time definitions	14/12/24	4	
24	CMOS Inverter design with delay constraints – Two sample mask lay out for p-type substrate. Unit-4: Static Combinational, Sequential, Dynamics logic circuits & Memories	20/12/24	6	} <i>SPK</i>
25	Define Static Combinational logic ,working of Static CMOS logic circuits (Two-input NAND Gate)	22/12/24	6	

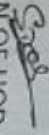
26	CMOS logic circuits ( NAND2 Gate)	23/12/21	5		
27	CMOS Transmission Gates(Pass gate)	27/12/21	5		
28	Complex Logic Circuits - Basics	28/12/21	5		
29	Classification of Logic circuits based on their temporal behaviour	29/12/21	6		
30	SR Flip latch Circuit,	6/1/22	4		
31	Clocked SR latch only.	10/1/22	6		
32	CMOS D latch.	11/1/22	5		
33	Basic principles of Dynamic Pass Transistor Circuits	13/1/22	4		
34	Dynamic RAM, SRAM,	17/1/22	6		
35	Flash memory	18/1/22	4		
	<b>Unit-5: System Design method &amp; synthesis</b>				
36	Design Language (SPL & HDL) & HDL & EDA tools & VHDL and packages Xilinx	19/1/22	6		
37	Design strategies & concept of FPGA with standard cell based design	20/1/22	6		
38	VHDL for design synthesis using CPLD or FPGA	24/1/22	5		
39	Raspberry Pi - Basic idea	25/1/22	4		
	<b>Unit-6: Introduction to Embedded Systems</b>				
40	Embedded Systems Overview, list of embedded systems, characteristics, example -- A Digital Camera	27/1/22	6		
41	Embedded Systems Technologies--Technology -- Definition -Technology for Embedded Systems -Processor Technology -IC Technology	31/1/22	6		
		27/2/22	-3		
42	Design Technology-Processor Technology, General Purpose Processors -- Software, Basic Architecture of Single Purpose Processors -- Hardware	3/2/22	6		
		7/2/22	6		
43	Application -- Specific Processors, Microcontrollers, Digital Signal Processors(DSP).	8/2/22	4		
44	IC Technology-- Full Custom / VLSI, Semi-Custom ASIC (Gate Array & Standard Cell), PLD (Programmable Logic Device)	10/2/22	6		
		21/2/22	6		
45	Basic idea of Arduino micro controller	23/2/22	6		
46	<b>QUESTIONS &amp; ANSWERS</b>	27/2/22	2		

SIGN OF FACULTY



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SIGN OF HOD



SIGN OF PRINCIPAL



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